PCI-4461 Feature Usage

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Contents

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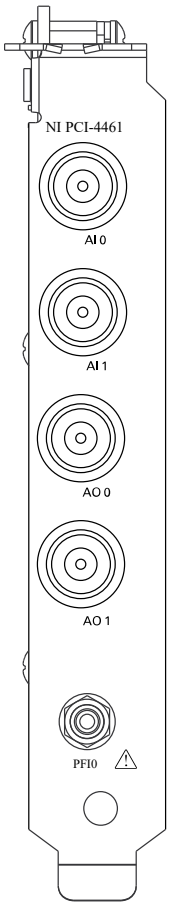
204.8 kS/s, 118 dB, 3.4 Hz AC/DC Coupled, 2-Input/2-Output Sound and Vibration Device

- 2 analog input channels; ±42.4 V; up to 204.8 kS/s simultaneous sampling rate
- 2 analog output channels; ±10 V; up to 204.8 kS/s update rate
- 24-bit resolution for good signal to noise ratio on AI channels
- Software-selectable IEPE signal conditioning (0 mA, 4 mA±15%, or 10 mA±15%)

PCI-4461 Pinout



The following figure shows the BNC connector polarity.

Figure 1. BNC Connector Polarity

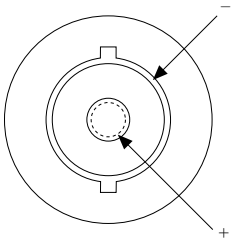


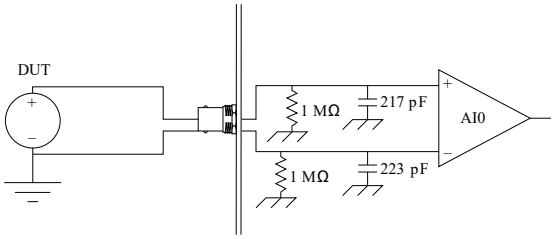
Table 1. Signal Descriptions

Signal	Reference	Description
AI <0,1>+, AI <0,1>-	—	Analog Input Channels—AI+ and AI- are the positive and negative inputs of the pseudodifferential or differential analog channel.
AO <0,1>+, AO <0,1>-	—	Analog Output Channels—AO+ and AO- are the positive and negative outputs of the pseudodifferential or differential analog channel.
PFI 0	GND	Programmable Function Interface—A digital trigger input.

Analog Input Connections

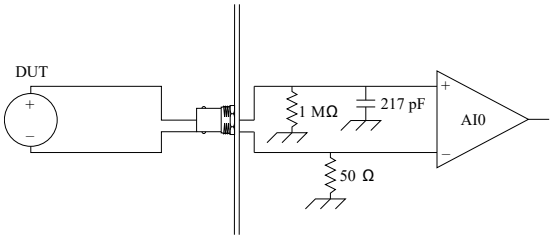
The following figure shows the PCI-4461 analog input connection in differential mode.

Figure 2. Input Connection in Differential Mode



The following figure shows the PCI-4461 analog input connection in pseudodifferential mode.

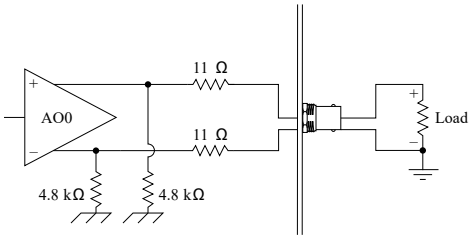
Figure 3. Input Connection in Pseudodifferential Mode



Analog Output Connections

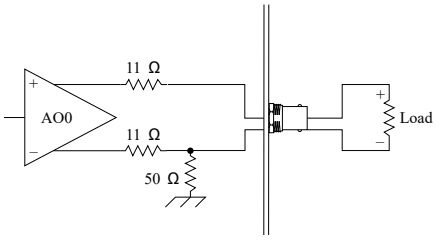
The following figure shows the PCI-4461 analog output connection in differential mode.

Figure 4. Output Connection in Differential Mode



The following figure shows the PCI-4461 analog output connection in pseudodifferential mode.

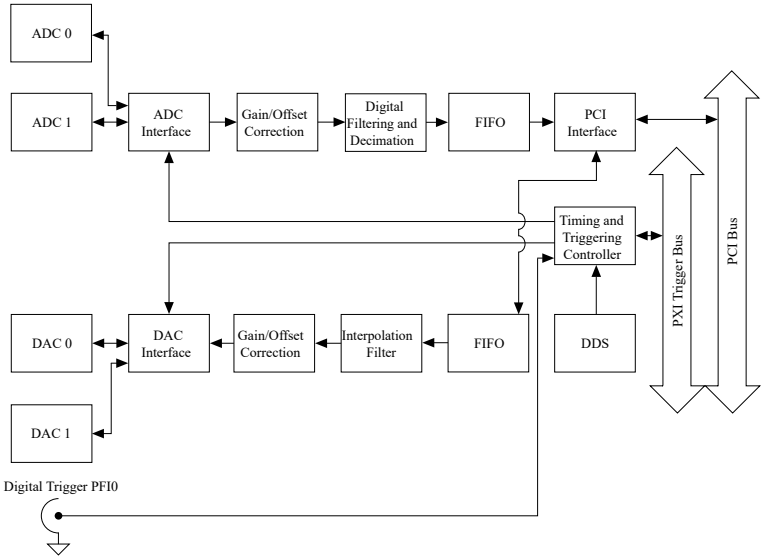
Figure 5. Output Connection in Pseudodifferential Mode



Block Diagram

The following figure shows the PCI-4461 block diagram.

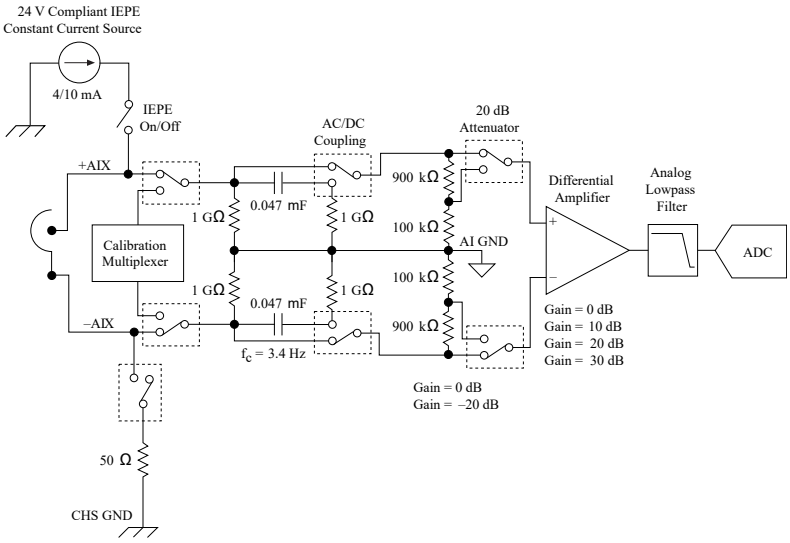
Figure 6. PCI-4461 Block Diagram



Analog Input Features

The following figure shows the PCI-4461 analog input circuitry block diagram.

Figure 7. Analog Input Block Diagram



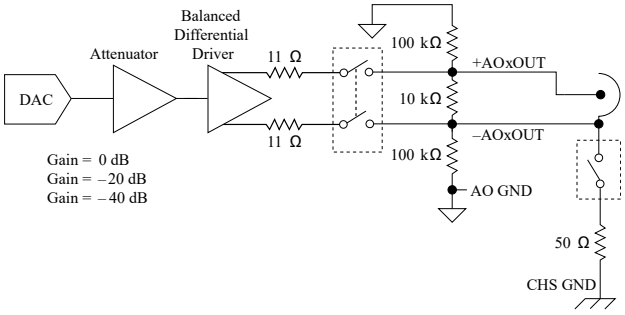
The PCI-4461 analog input channels feature the following:

- Sampling rates up to 204.8 kS/s
- Per channel selection of six input voltage ranges from ±0.316 V to ±42.4 V pk
- Per channel differential and pseudodifferential channel configuration
- Per channel AC or DC coupling
- Per channel IEPE current excitation
- Pre-digitization and post-digitization overload detection
- Anti-alias filtering
- Multiple triggering modes, including external digital triggering

Analog Output Features

The following figure shows the PCI-4461 analog output circuitry block diagram.

Figure 8. Analog Output Block Diagram



The PCI-4461 analog output channels feature the following:

- Update rates to 204.8 kS/s
- Per channel selection of three output voltages of ±10 V, ±1 V, or ±0.1 V
- Per channel differential and pseudodifferential channel configuration
- Anti-image filtering
- External digital triggering

Gain and Attenuation

Positive gain values amplify the signal before the A/D converter (ADC) digitizes it. This signal amplification reduces the measurement range. However, amplifying the signal before digitization allows better resolution by strengthening weak signal components before they reach the ADC. Conversely, negative gains attenuate the signal before they reach the ADC. This attenuation increases the effective measurement range, though it

sacrifices dynamic range for weaker signal components.

In this manual, AI attenuation is referred to as gain with a negative value. You can set attenuation directly in software by assigning a negative value to the AI.Gain property. Refer to the ***NI-DAQmx Help*** or the ***LabVIEW Help*** for more information.

The PCI-4461 has six available gain settings for each AI channel. Each gain setting corresponds to a particular AI range, and each range is centered on 0 V. The gain settings are specified in decibels, where the 0 dB reference is the default input range of ±10 V. Refer to the specifications for your device or module for detailed information about each gain setting and corresponding range.

The range for the -20 dB setting corresponds to a maximum input range of ±42.4 V pk. Setting the gain to -20 dB attenuates the signal by a factor of 10, implying a maximum ADC range of ±100 V. However, the analog front-end circuitry is not rated beyond ±42.4 V pk. When you use this gain setting, the ADC does not saturate at ±42.4 V pk; however, you risk damaging the measurement system or creating a possible safety hazard if you exceed the maximum rated input of ±42.4 V pk.

The following table shows the gain setting sources.

Table 2. Gain Setting Sources

Gain Setting (dB)	Source
0, 10, 20, 30	Differential amplifier
-10	Combination of -20 and 10 gains
-20	Resistor divider network

In general, select the voltage range that provides the greatest dynamic range and the least distortion. For example, consider an accelerometer with a 100 mV/g sensitivity rating with a maximum acceleration measurement range of 50 g peak. This would correspond to a maximum output voltage of 5 Vpk. In this case, the ±10 V pk is appropriate, corresponding to 0 dB gain. However, the ±3.16 Vpk setting maximizes the dynamic range if you know, for example, that the stimulus is limited to 20 g or 2 Vpk.

Minimize system distortion by providing sufficient headroom between the stimulus setting, 2 Vpk in this instance, and the range. Choose the next highest range setting

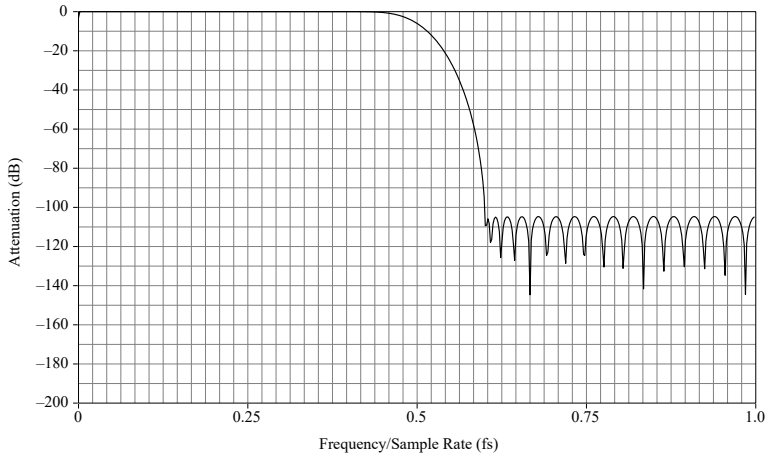
above the peak level you expect to measure to provide sufficient headroom. In applications where distortion performance is critical, you can sacrifice overall dynamic range to improve distortion performance by selecting the ±10 V pk setting. Refer to the specifications for your device or module for distortion specifications for each gain setting.

The ADC is the most significant source of measurement noise until you use the 20 dB or 30 dB gain settings. At these higher gain settings, the analog front-end circuitry becomes the dominant noise source. To achieve the best absolute noise performance, select the highest gain setting appropriate for your application.

Anti-Aliasing Filter Response

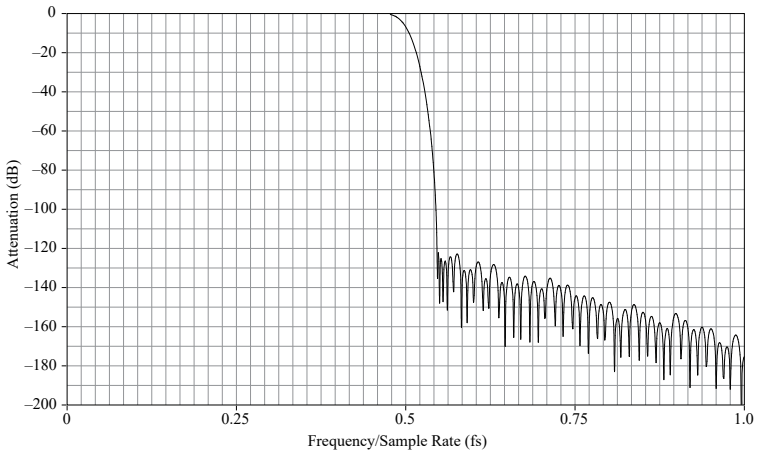
The following figure shows the digital filter input frequency response with low-frequency alias rejection enabled.

Figure 9. Digital Filter Input Frequency Response with Low-Frequency Alias Rejection Enabled



The following figure shows the digital filter input frequency response with low-frequency alias rejection disabled.

Figure 10. Digital Filter Input Frequency Response with Low-Frequency Alias Rejection Disabled

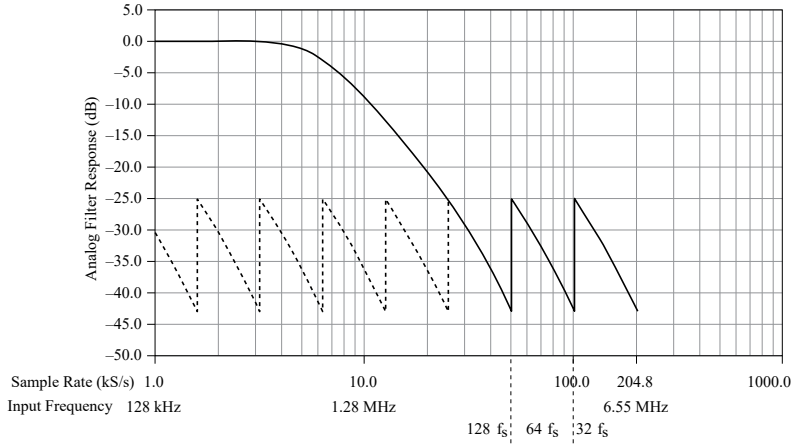


The following figure shows the response of the analog anti-aliasing filter with and without enhanced low-frequency alias rejection enabled. The following figure illustrates the alias rejection for a tone that passes the digital filter by falling into one of the f_S-wide bands centered on the oversample rate. The first set of x-axis labels denotes the PCI-4461 sample rate in kS/s. The second set of x-axis labels shows the frequency of an input signal that could pass through the digital filter at the given sampling rate. Refer to the ***ADC Modulator Oversample Rate*** in the specifications for your device or module for more information.

For example, when sampling at 10 kS/s, the digital filter will remove any out-of-bandwidth tones up to a 10 kHz band centered on 128 f_S, or 1.28 MHz±5 kHz. If noise in the input signal falls into this narrow window, the noise is not rejected by the digital filter. In this limited frequency range, you must consider the analog filter. The following figure illustrates that with a sampling rate of 10 kS/s, the analog filter attenuates an input signal frequency of 1.28 MHz by -9 dB without enhanced low-frequency alias rejection enabled. With enhanced low-frequency alias rejection enabled, the attenuation would be -36 dB.

The sawtooth line in the following figure represents the filter response with low-frequency alias rejection enabled. The worst-case alias rejection is approximately -25 dB. This corresponds to the analog filter attenuation at 25.6 kS/s.

Figure 11. Analog Filter Input Frequency Response



This situation represents the worst-case alias rejections for each sampling rate. You would only observe this worst-case scenario with a well-defined tone in a narrow frequency range. In real measurement situations, it is more likely that any energy passing the digital filter consists only of low-amplitude noise. If an unwanted component does appear in the digitized signal, increasing the sampling rate might provide an easy solution by both improving the rejection from the analog filter and by repositioning the digital filter so that it can eliminate the alias.

Reference Clock Synchronization

The PCI-4461 employs onboard PLL circuitry. The PLL circuitry locks the onboard 100 MHz voltage-controlled crystal oscillator (VCXO) to the PXI 10 MHz reference clock signal, PXI_CLK10. The VCXO output provides the source for the DDS chip, which generates the sample clock timebase. In this way the PCI-4461 locks the sample clock timebase to PXI_CLK10.