PXIe-1095 User Manual

2025-03-26

Contents

PXIe-1095 Chassis Manual

The PXIe-1095 chassis combines a high-performance 18-slot PXI Express backplane with a high-output power supply and a structural design that has been optimized for maximum usability in a wide range of applications. The chassis' modular design ensures a high level of maintainability, resulting in a very low mean time to repair (MTTR). The PXIe-1095 chassis fully complies with the ***PXI-5 PXI Express Hardware Specification***, offering advanced timing and synchronization features.

An optional timing and synchronization upgrade provides inter-chassis trigger routing capability, higher accuracy CLK10 and CLK100, connectors for 10 MHz reference clock input and output, and remote chassis monitoring and inhibit control.

The key features of the PXIe-1095 chassis include the following:

Related reference:

- Chassis Components
- Pinouts
- LED Indicators
- DIP Switches
- Backplane Overview
- PXIe-1095 Installation
- PXIe-1095 Configuration
- Maintenance
- Calibration

High Performance for Instrumentation Requirements

- Up to 8 GB/s (single direction) per PXI Express slot dedicated bandwidth (x8 Gen-3 PCI Express).
- 58 W per slot cooling from 0 °C to 55 °C, and 82 W per slot cooling from 0 °C to 40 °C, meets increased PXI Express cooling requirements
- Low-jitter internal 10 MHz reference clock for PXI/PXI Express slots with ± 25 ppm stability

- Low-jitter internal 100 MHz reference clock for PXI Express slots with ± 25 ppm stability
- Quiet operation for 0 to 30 °C at 37.7 dBA
- Variable speed fan controller optimizes cooling and acoustic emissions
- Complies with PXI and CompactPCI Specifications

High Reliability

- 0 to 55 °C extended temperature range
- Power supply, temperature, and fan monitoring
- Field replaceable fans
- Dual redundant, hot-swappable power supplies

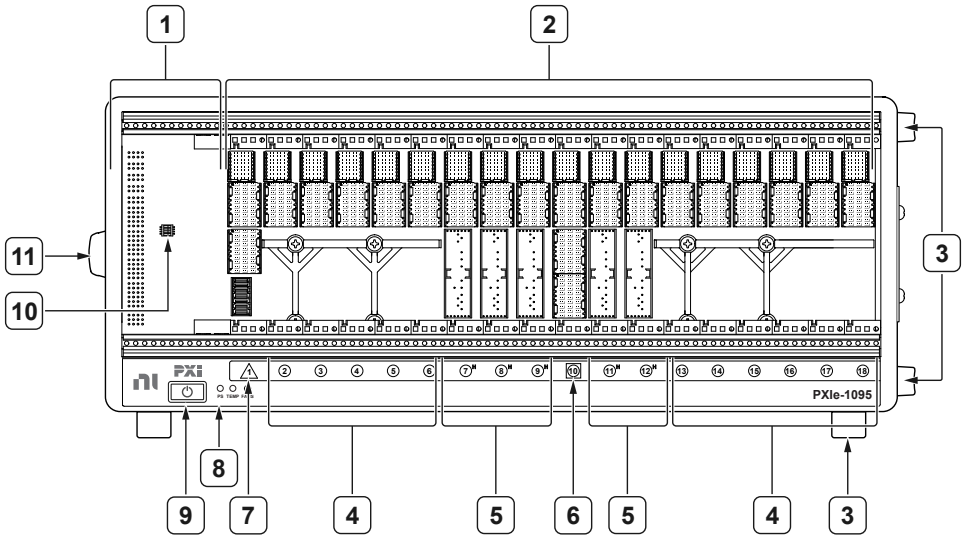
Multi-Chassis Support

- PXI Express System Timing Slot for tight synchronization across multiple chassis
- Switchless CLK10 routing

Chassis Components

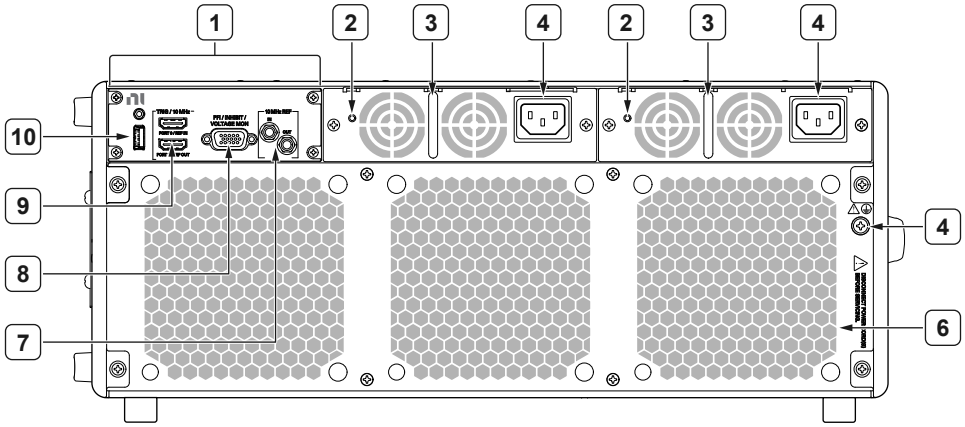
The following figures show key features of the PXIe-1095 chassis front and back panels.

Figure 1. Front View of the PXIe-1095



1. System Controller Expansion Slot
2. Backplane Connectors
3. Removable Feet
4. PXI Express Peripheral Slots (11x)
5. PXI Express Hybrid Peripheral Slots (5x)
6. PXI Express System Timing Slot
7. PXI Express System Controller Slot
8. Front Panel LEDs
9. Power Inhibit Switch
10. DIP Switch
11. Chassis Carry Handle

Figure 2. Rear View of the PXIe-1095



1. Timing and Synchronization Upgrade
2. Rear Panel Power Supply LED
3. Power Supply
4. Universal AC Input
5. Chassis Protective Earth Terminal
6. Fan Module
7. 10 MHz REF IN and OUT SMA Female Connectors
8. Remote Inhibit and Chassis Monitoring Port
9. High-Density Trigger Ports
10. USB 3.0 Port

Optional Equipment

Contact NI to order the following options for the PXIe-1095 chassis.

- **EMC Filler Panels**—EMC filler panel kits are available from NI.
- **Rack Mount Kits**—Rack mounting kits are available from NI that can accommodate a variety of rack depths.
- **Slot Blockers**—PXI Slot Blocker kits are available from NI for improved thermal performance when all slots are not used.
- **Replacement Power Supply**—Replacement power supply kits are available from NI.
- **Replacement Fan Kit**—A fan kit available from NI includes both side and PXI module fan assemblies.

Related reference:

- Installing Filler Panels
- Rack Mounting
- Installing Slot Blockers
- Replacing the Power Supply
- Installing Replacement Fan Assemblies

Pinouts

This section describes the connector pinouts for the PXIe-1095 chassis backplane.

System Controller Slot XP1 Connector Pinout

Pins	Signals
A	GND
B	12V
C	12V
D	GND
E	5V
F	3.3V
G	GND

System Controller Slot XP2 Connector Pinout

Pin	A	B	ab	C	D	cd	E	F	ef
1	2PETp1	2PETn1	GND	2PERp1	2PERn1	GND	2PETp2	2PETn2	GND
2	2PETp3	2PETn3	GND	2PERp3	2PERn3	GND	2PERp2	2PERn2	GND
3	2PETp4	2PETn4	GND	2PERp4	2PERn4	GND	2PETp5	2PETn5	GND
4	2PETp6	2PETn6	GND	2PERp6	2PERn6	GND	2PERp5	2PERn5	GND
5	2PETp7	2PETn7	GND	2PERp7	2PERn7	GND	2PETp8	2PETn8	GND
6	2PETp9	2PETn9	GND	2PERp9	2PERn9	GND	2PERp8	2PERn8	GND
7	2PETp10	2PETn10	GND	2PERp10	2PERn10	GND	2PETp11	2PETn11	GND
8	2PETp12	2PETn12	GND	2PERp12	2PERn12	GND	2PERp11	2PERn11	GND
9	2PETp13	2PETn13	GND	2PERp13	2PERn13	GND	2PETp14	2PETn14	GND
10	2PETp15	2PETn15	GND	2PERp15	2PERn15	GND	2PERp14	2PERn14	GND

System Controller Slot XP3 Connector Pinout

Pin	A	B	ab	C	D	cd	E	F	ef
1	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND

Pin	A	B	ab	C	D	cd	E	F	ef
2	RSV	RSV	GND	PWR_OK	PS_ON#	GND	LINKCAP	PWRBTN#	GND
3	SMBDAT	SMBCLK	GND	RSVD	RSVD	GND	RSVD	RSVD	GND
4	RSV	PERST#	GND	2RefClk+	2RefClk-	GND	1RefClk+	1RefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	2PETp0	2PETn0	GND	2PERp0	2PERn0	GND	1PERp7	1PERn7	GND

System Controller Slot XP4 Connector Pinout

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	RSV	RSV	RSV	RSV	RSV	GND
4	GND	RSV	RSV	RSV	RSV	RSV	GND
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
6	GND	PXI_TRIG2	GND	RSV	PXI_STAR	PXI_CLK10	GND
7	GND	PXI_TRIG1	PXI_TRIG0	RSV	GND	PXI_TRIG7	GND
8	GND	RSV	GND	RSV	RSV	PXI_LBR6	GND

System Timing Slot TP1 Connector Pinout

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_ DSTARA3+	PXIe_ DSTARA3-	GND	PXIe_ DSTARC7+	PXIe_ DSTARC7-	GND	PXIe_ DSTARC12+	PXIe_ DSTARC12-	GND
2	PXIe_ DSTARC4+	PXIe_ DSTARC4-	GND	PXI_ STAR12	PXI_ STAR13	GND	PXIe_ DSTARA12+	PXIe_ DSTARA12-	GND

Pin	A	B	ab	C	D	cd	E	F	ef
3	PXIe_ DSTARB4+	PXIe_ DSTARB4-	GND	PXIe_ DSTARA16+	PXIe_ DSTARA16-	GND	PXIe_ DSTARB12+	PXIe_ DSTARB12-	GND
4	PXIe_ DSTARA4+	PXIe_ DSTARA4-	GND	PXIe_ DSTARB7+	PXIe_ DSTARB7-	GND	PXIe_ DSTARC13+	PXIe_ DSTARC13-	GND
5	PXIe_ DSTARC5+	PXIe_ DSTARC5-	GND	PXI_ STAR14	PXI_ STAR15	GND	PXIe_ DSTARA13+	PXIe_ DSTARA13-	GND
6	PXIe_ DSTARB5+	PXIe_ DSTARB5-	GND	PXIe_ DSTARB16+	PXIe_ DSTARB16-	GND	PXIe_ DSTARB13+	PXIe_ DSTARB13-	GND
7	PXIe_ DSTARA5+	PXIe_ DSTARA5-	GND	PXIe_ DSTARA7+	PXIe_ DSTARA7-	GND	PXIe_ DSTARC14+	PXIe_ DSTARC14-	GND
8	PXIe_ DSTARC6+	PXIe_ DSTARC6-	GND	PXI_ STAR16	RSV	GND	PXIe_ DSTARA14+	PXIe_ DSTARA14-	GND
9	PXIe_ DSTARB6+	PXIe_ DSTARB6-	GND	PXIe_ DSTARC15+	PXIe_ DSTARC15-	GND	PXIe_ DSTARB14+	PXIe_ DSTARB14-	GND
10	PXIe_ DSTARA6+	PXIe_ DSTARA6-	GND	PXIe_ DSTARB15+	PXIe_ DSTARB15-	GND	PXIe_ DSTARA15+	PXIe_ DSTARA15-	GND

System Timing Slot TP2 Connector Pinout

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_ DSTARC0+	PXIe_ DSTARC0-	GND	PXIe_ DSTARC8+	PXIe_ DSTARC8-	GND	PXIe_ DSTARB8+	PXIe_ DSTARB8-	GND

Pin	A	B	ab	C	D	cd	E	F	ef
2	PXIe_ DSTARA0+	PXIe_ DSTARA0-	GND	PXIe_ DSTARC9+	PXIe_ DSTARC9-	GND	PXIe_ DSTARA8+	PXIe_ DSTARA8-	GND
3	PXIe_ DSTARB0+	PXIe_ DSTARB0-	GND	PXIe_ DSTARC1+	PXIe_ DSTARC1-	GND	PXIe_ DSTARA9+	PXIe_ DSTARA9-	GND
4	PXIe_ DSTARB1+	PXIe_ DSTARB1-	GND	PXI_ STAR0	PXI_ STAR1	GND	PXIe_ DSTARB9+	PXIe_ DSTARB9-	GND
5	PXIe_ DSTARA1+	PXIe_ DSTARA1-	GND	PXI_ STAR2	PXI_ STAR3	GND	PXIe_ DSTARC10+	PXIe_ DSTARC10-	GND
6	PXIe_ DSTARC2+	PXIe_ DSTARC2-	GND	PXI_ STAR4	PXI_ STAR5	GND	PXIe_ DSTARA10+	PXIe_ DSTARA10-	GND
7	PXIe_ DSTARB2+	PXIe_ DSTARB2-	GND	PXI_ STAR6	PXI_ STAR7	GND	PXIe_ DSTARB10+	PXIe_ DSTARB10-	GND
8	PXIe_ DSTARA2+	PXIe_ DSTARA2-	GND	PXI_ STAR8	PXI_ STAR9	GND	PXIe_ DSTARC11+	PXIe_ DSTARC11-	GND
9	PXIe_ DSTARC3+	PXIe_ DSTARC3-	GND	PXI_ STAR10	PXI_ STAR11	GND	PXIe_ DSTARA11+	PXIe_ DSTARA11-	GND
10	PXIe_ DSTARB3+	PXIe_ DSTARB3-	GND	PXIe_ DSTARC16+	PXIe_ DSTARC16-	GND	PXIe_ DSTARB11+	PXIe_ DSTARB11-	GND

System Timing Slot XP3 Connector Pinout

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_ CLK100+	PXIe_ CLK100-	GND	PXIe_ SYNC100+	PXIe_ SYNC100-	GND	PXIe_ DSTARC+	PXIe_ DSTARC-	GND
2	PRSNT#	PWREN#	GND	PXIe_ DSTARB+	PXIe_ DSTARB-	GND	PXIe_ DSTARA+	PXIe_ DSTARA-	GND
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND
4	MPWRGD*	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND

System Timing Slot XP4 Connector Pinout

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	12V	12V	GND	GND	GND	GND
4	GND	GND	GND	3.3V	3.3V	3.3V	GND
5	GND	PXI_ TRIG3	PXI_ TRIG4	PXI_ TRIG5	GND	PXI_ TRIG6	GND
6	GND	PXI_ TRIG2	GND	ATNLED	PXI_ CLK10_IN	PXI_ CLK10	GND
7	GND	PXI_	PXI_	ATNSW#	GND	PXI_	GND

Pin	Z	A	B	C	D	E	F
		TRIG1	TRIG0			TRIG7	
8	GND	PXIe_ SYNC_CTRL	GND	RSV	PXI_ LBL6	PXI_ LBR6	GND

Hybrid Slot P1 Connector Pinout

Pin	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12 to 14	Key Area						
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND

Pin	Z	A	B	C	D	E	F
4	GND	IPMB_PWR	HEALTHY#	# V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

Hybrid Slot XP3 Connector Pinout

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_ CLK100+	PXIe_ CLK100-	GND	PXIe_ SYNC100+	PXIe_ SYNC100-	GND	PXIe_ DSTARC+	PXIe_ DSTARC-	GND
2	PRSNT#	PWREN#	GND	PXIe_ DSTARB+	PXIe_ DSTARB-	GND	PXIe_ DSTARA+	PXIe_ DSTARA-	GND
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND
4	MPWRGD*	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND

Hybrid Slot XP4 Connector Pinout

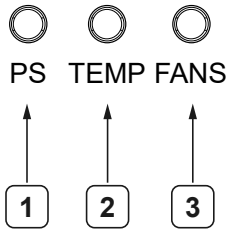
Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	12V	12V	GND	GND	GND	GND
4	GND	GND	GND	3.3V	3.3V	3.3V	GND

Pin	Z	A	B	C	D	E	F
5	GND	PXI_ TRIG3	PXI_ TRIG4	PXI_ TRIG5	GND	PXI_ TRIG6	GND
6	GND	PXI_ TRIG2	GND	ATNLED	PXI_ STAR	PXI_ CLK10	GND
7	GND	PXI_ TRIG1	PXI_ TRIG0	ATNSW#	GND	PXI_ TRIG7	GND
8	GND	RSV	GND	RSV	PXI_ LBL6	PXI_ LBR6	GND

LED Indicators

The following figure shows the front panel LEDs. The following table describes the LED states.

Figure 3. Front Panel LEDs



1. Power Supply LED
2. Temperature LED
3. Fan LED

Table 1. Front Panel LED States

LED	State	Description
Power Supply LED	Off	Chassis is powered off.
	Steady green	Chassis power supply or supplies are active, and operating normally.
	Blinking red	In a redundant power setup, one power supply has failed.
	Steady red	The chassis power supply or supplies have failed.
Temperature LED	Off	Chassis is powered off.
	Steady green	Intake or exhaust temperature is within chassis operating range.
	Steady red	Intake or exhaust temperature is outside of chassis operating range.
Fan LED	Off	Chassis is powered off.

LED	State	Description
	Steady green	All chassis fans are enabled and operating normally.
	Steady red	One or more chassis fans have failed.
All LEDs	Blinking red	An internal chassis fault has occurred.

The chassis power supply has a single LED that indicates the health of that supply. The following table describes the rear panel LED states. Refer to the ***Rear View of the PXIe-1095*** figure in the Chassis Components topic for the LED location.

Table 2. Rear Power Supply LED States

State	Description
Off	Power supply is unplugged or in standby.
Steady green	Main power is active and supply is operating normally.
Blinking red	Power supply is operating outside of specification.
Steady red	Power supply has failed.

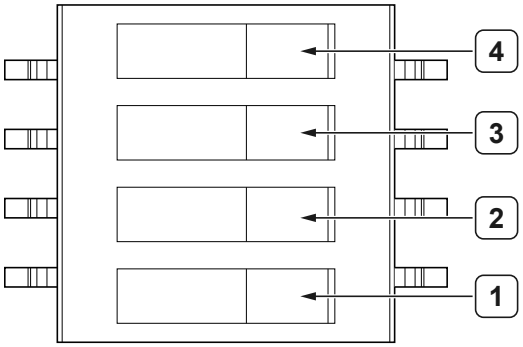
DIP Switches

The backplane has a DIP switch that may be used to control chassis behavior.

DIP switch #1 (first from the left) controls the chassis fan mode. When this switch is in the off (down) position, Auto mode is selected. When this switch is in the on (up) position, High mode is selected.

DIP switch #2 (second from the left) controls the chassis Inhibit Mode. When this switch is in the off (down) position, Default mode is selected. When this switch is in the on (up) position, Manual mode is selected.

Figure 4. Backplane DIP Switches



1. Switch #1 (Fan)
2. Switch #2 (PWR)
3. Switch #3 (NC)
4. Switch #4 (NC)

Table 3. DIP Switch States

Location	Switch	State	Description
1	FAN	Off (Right)	Sets chassis Fan Mode to Auto.
		On (Left)	Sets chassis Fan Mode to High.
2	PWR	Off (Right)	Sets chassis Inhibit Mode to Default.
		On (Left)	Sets chassis Inhibit

Location	Switch	State	Description
			Mode to Manual.
3	NC	—	—
4	NC	—	—

Backplane Overview

The following topics provide an overview of the backplane features for the PXIe-1095 chassis.

Interoperability with CompactPCI

The design of the PXIe-1095 provides you the flexibility to use the following devices in a single PXI Express chassis:

- PXI Express compatible products
- CompactPCI Express compatible 2-Link system controller products
- CompactPCI Express compatible Type-2 peripheral products
- PXI peripheral products modified to fit in a hybrid slot
- Standard CompactPCI peripheral products modified to fit in a hybrid slot

System Controller Slot

The system controller slot is slot 1 of the chassis and is a 2-Link configuration system slot as defined by the CompactPCI Express and PXI Express specifications. The chassis includes three system controller expansion slots for system controller modules that are wider than one slot. These slots allow the system controller to expand to the left to prevent the system controller from using peripheral slots.

The backplane connects the system slot to two PCI Express switches using a Gen-3 x8 link and a Gen-3 x16 link. The two PCIe switches distribute PCIe links to the peripheral slots and to a PCIe-to-PCI bridge to provide a PCI bus to the hybrid peripheral slots.

System slot link 1 is a Gen-3 x8 PCI Express link to the first PCI Express switch, providing a nominal bandwidth of 8 GB/s (single direction) between the system controller and PCI Express switch 1. PXI Express peripheral slots 2-10 are connected to PCI Express switch 1 with Gen-3 x8 PCI Express links and are downstream of system slot link 1.

System slot link 2 is a Gen-3 x16 PCI Express link to the second PCI Express switch,

providing a nominal bandwidth of 16 GB/s (single direction) between the system controller slot and PCI Express switch 2. PXI Express peripheral slots 11-18 are connected to PCI Express switch 2 with Gen-3 x8 PCI Express links and are downstream of system slot link 2.

The PCI Express-to-PCI bridge is connected to PCI Express switch 1 and provides a 32-bit, 33 MHz PCI bus for hybrid peripheral slots 7, 8, 9, 11, and 12.

The system controller slot also has connectivity to some PXI features such as: PXI_CLK10, PXI Star, PXI Trigger Bus, and PXI Local Bus 6. By default, the system controller controls the power supply with the PS_ON# signals. A logic low on this line powers on the power supply.

Note The chassis Inhibit Mode must be set to Default mode for the system controller to control the power supply. Refer to the ***Inhibit Mode*** section for details about configuring Inhibit Mode.

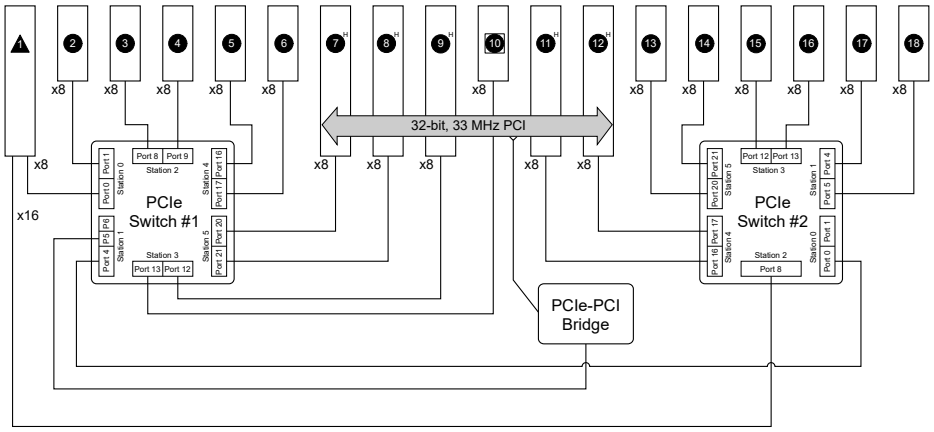
Hybrid Peripheral Slots

The chassis provides five (5) hybrid peripheral slots as defined by the ***PXI-5 PXI Express Hardware Specification***: slots 7, 8, 9, 11, and 12. A hybrid peripheral slot can accept the following peripheral modules:

- A PXI Express peripheral with x8, x4, or x1 PCI Express link through a switch to the system slot.
- A CompactPCI Express Type-2 Peripheral with x8, x4, or x1 PCI Express link through a PCI Express switch to the system slot.
- Each PXI Express or CompactPCI Express peripheral can link to Gen-3 8.0 GT/s x8 with the PCI Express interface, providing a maximum nominal single-direction bandwidth of 8 GB/s.
- A hybrid-compatible PXI Peripheral module modified by replacing the J2 connector with an XJ4 connector installed in the upper eight rows of J2. Refer to the ***PXI Express Specification*** for details. The PXI peripheral communicates through the backplane's 32-bit PCI bus.
- A CompactPCI 32-bit peripheral on the backplane's 32-bit PCI bus.

The hybrid peripheral slots provide full PXI Express functionality and 32-bit PXI functionality except for PXI Local Bus. The hybrid peripheral slot only connects to PXI Local Bus 6 left and right.

Figure 5. PXIe-1095 PCI Express Backplane Diagram

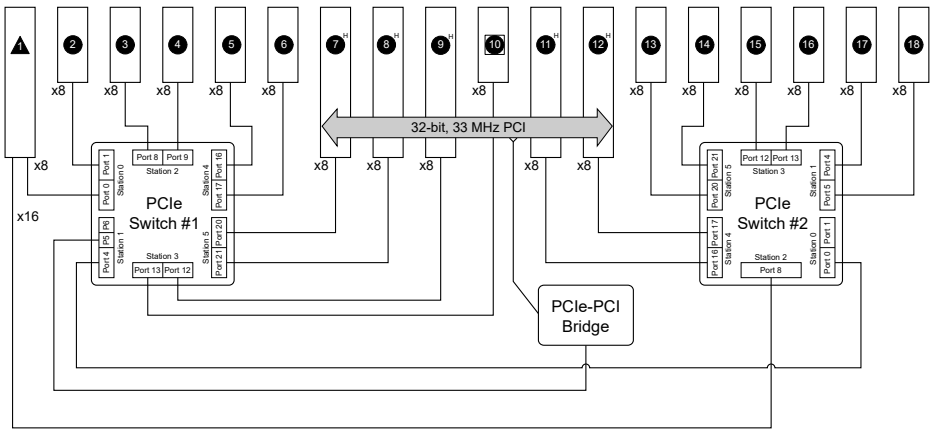


PXI Express Peripheral Slots

There are eleven (11) PXI Express peripheral slots: slots 2 to 6 and 13 to 18. PXI Express peripheral slots can accept the following modules:

- A PXI Express Peripheral with x8, x4, or x1 PCI Express link to the system slot or through a PCI Express switch.
- A CompactPCI Express Type-2 Peripheral with x8, x4, or x1 PCI Express link to the system slot or through a PCI Express switch.
- Each PXI Express or CompactPCI Express peripheral can link to Gen-3 8.0 GT/s x8 with the PCI Express interface, providing a maximum nominal single-direction bandwidth of 8 GB/s.

Figure 6. PXIe-1095 PCI Express Backplane Diagram



System Timing Slot

The system timing slot is slot 10. The system timing slot accepts the following peripheral modules:

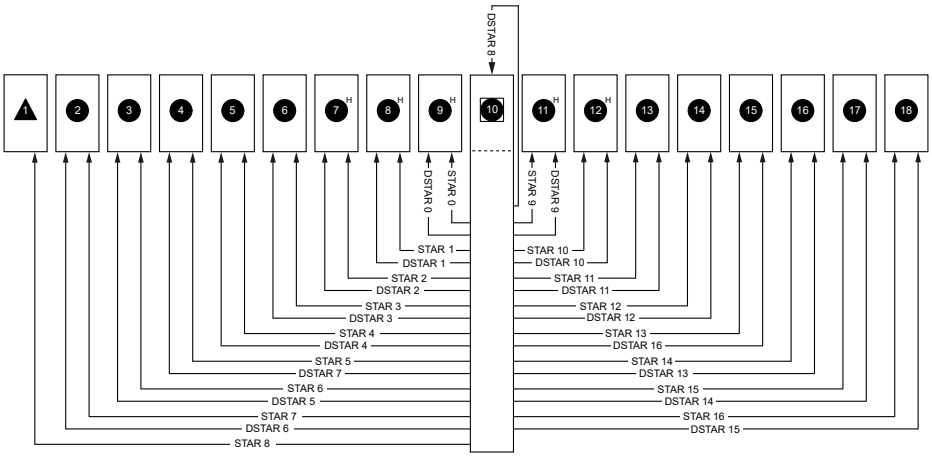
- A PXI Express System Timing Module with x8, x4, or x1 PCI Express link to the system slot through a PCI Express switch. Each PXI Express peripheral or hybrid peripheral slot can link up to a Gen-3 x8 PCI Express, providing a maximum nominal single-direction bandwidth of 8 GB/s.
- A PXI Express Peripheral with x8, x4, or x1 PCI Express link to the system slot through a PCI Express switch.
- A CompactPCI Express Type-2 Peripheral with x8, x4, or x1 PCI Express link to the system slot through a PCI Express switch.

The system timing slot has three (3) dedicated differential pairs (PXIe_DSTAR) connected from the TP1 and TP2 connectors to the XP3 connector for each PXI Express hybrid peripheral slot, as well as routed back to the XP3 connector of the system timing slot, as shown in the following figure. You can use the PXIe_DSTAR pairs for high-speed triggering, synchronization, and clocking. Refer to the ***PXI Express Specification*** for details.

The system timing slot also has a single-ended (PXI Star) trigger connected to every slot. Refer to the following figure for more details.

The system timing slot has a pin (PXI_CLK10_IN) through which a system timing module may source a 10 MHz clock to which the backplane phase-locks.

Figure 7. PXI Express Star Connectivity Diagram



PXI Local Bus

The PXI backplane local bus is a daisy-chained bus that connects each peripheral slot with adjacent peripheral slots to the left and right.

The backplane routes PXI Local Bus 6 between all slots. The left local bus 6 from slot 1 is not routed anywhere, and the right local bus 6 from slot 18 is not routed anywhere.

Local bus signals may range from high-speed TTL signals to analog signals as high as 42 V.

Initialization software uses the configuration information specific to each adjacent peripheral module to evaluate local bus compatibility.

PXI Trigger Bus

All slots on the same PXI bus segment share eight PXI trigger lines. You can use these trigger lines in a variety of ways. For example, you can use triggers to synchronize the operation of several different PXI peripheral modules. In other applications, one module located in the system timing slot can control carefully timed sequences of operations performed on other modules in the system. Modules can pass triggers to one another on the lines, allowing precisely timed responses to asynchronous external events the system is monitoring or controlling.

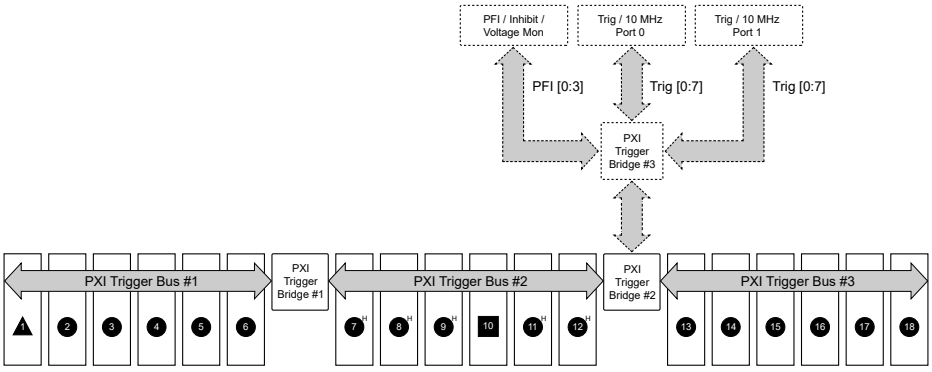
The PXI trigger lines from adjacent PXI trigger bus segments can be routed in either

direction across the PXI trigger bridges through buffers. This allows you to send trigger signals to, and receive trigger signals from, every slot in the chassis. Static trigger routing (user-specified line and directional assignments) can be configured through Measurement & Automation Explorer (MAX). Dynamic routing of triggers (automatic line assignments) is supported through certain NI drivers like NI-DAQmx.

Note Although any trigger line may be routed in either direction, it cannot be routed in more than one direction at a time.

With the Timing and Synchronization upgrade, PXI trigger lines can also be routed to I/O ports on the rear of the chassis. This allows you to send trigger signals to, and receive trigger signals from, devices in other chassis. NI drivers such as NI-DAQmx must be used to route triggers between chassis dynamically; routing triggers between chassis using static routes defined in MAX is not supported.

Figure 8. PXI Trigger Bus Connectivity Diagram

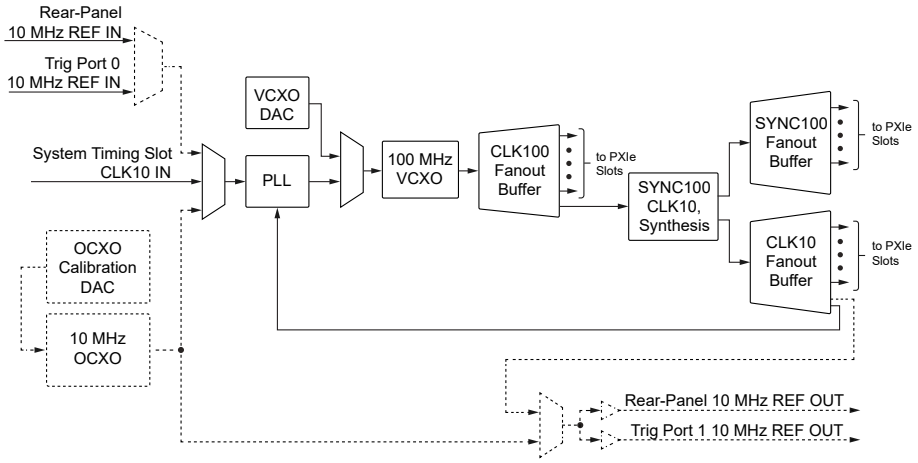


Note Dotted line connections are available only with the Timing and Synchronization upgrade.

System Reference Clock

The PXIe-1095 chassis supplies PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 to every peripheral slot with an independent driver for each signal. The following figure shows the chassis reference clock architecture.

Figure 9. Chassis Reference Clock Architecture



Note Dotted line connections are available only with the Timing and Synchronization upgrade.

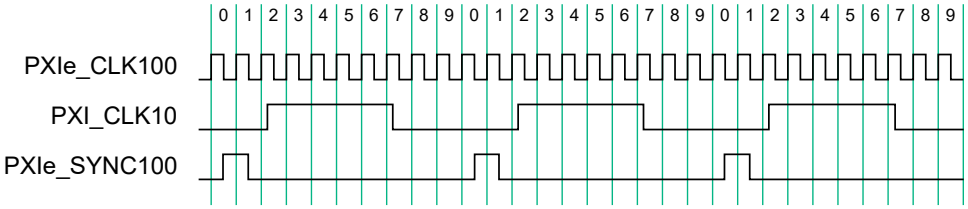
An independent buffer (having a source impedance matched to the backplane and a skew of less than 250 ps between slots) drives PXI_CLK10 to each slot. You can use this common reference clock signal to synchronize multiple modules in a measurement or control system.

An independent buffer drives PXIe_CLK100 to each peripheral slot. These clocks are matched in skew to less than 100 ps. The differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe_CLK100 so that when there is no peripheral or a peripheral that does not connect to PXIe_CLK100, there is no clock being driven on the pair to that slot. Refer to the following figure for a termination example.

An independent buffer drives PXIe_SYNC100 to each peripheral slot. The differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe_SYNC100 so that when there is no peripheral or a peripheral that does not connect to PXIe_SYNC100, there is no SYNC100 signal being driven on the pair to that slot.

The backplane uses a 100 MHz Voltage-Controlled Crystal Oscillator (VCXO) to directly create PXIe_CLK100 and does a divide-by-10 to create PXI_CLK10. Onboard logic synthesizes PXIe_SYNC100 from these two signals with the timing relationship as shown in the following figure.

Figure 10. System Reference Clock Default Behavior



This architecture has the advantage that PXI_CLK10 and PXIe_CLK100 are always sourced from the same reference oscillator, and therefore it is impossible to lose PXI_CLK10 or PXIe_CLK100 by disconnecting a reference provided on any of the supported inputs. For the same reason, it is also impossible for a runt pulse or glitch to occur on these lines as references are switched in and out, protecting the integrity of digital circuitry operating on these clocks.

A feature of this architecture is that the phase noise performance of PXI_CLK10 and PXIe_CLK100 is fixed beyond the bandwidth of the PLL loop on the backplane, regardless of the quality of reference used. This is advantageous if a reference with poor phase noise performance is used, but it also means that supplying a high end, low phase noise reference will not greatly improve PXI_CLK10 or PXIe_CLK100.

Related reference:

- OCXO
- 10 MHz Input Reference
- 10 MHz Output Reference

OCXO

With the Timing and Synchronization upgrade, the chassis has an internal precision 10 MHz Oven-Controlled Crystal Oscillator (OCXO) that serves as the default reference for the backplane PLL. The user can still provide a 10 MHz reference via any of the supported input ports if a different reference signal is needed.

The main source of frequency error in reference oscillators is temperature variation. An OCXO minimizes this error by housing the crystal oscillator circuit inside a sealed oven, which is maintained at a constant temperature higher than the ambient temperature external to the OCXO. This results in a reference oscillator that is several orders of magnitude more stable and accurate than regular crystal oscillators.

Because the OCXO must warm up to a higher temperature than the ambient temperature around it, there is a warm up time required to achieve the specified frequency accuracy. For this reason, to achieve the most stable operation of the OCXO, avoid powering off the OCXO.

The OCXO that the PXIe-1095 uses features electronic frequency control. This allows the OCXO to be fine-tuned by varying the control voltage to the OCXO. The chassis uses a 16-bit digital-to-analog converter (DAC) to give precise control of the tuning voltage. The PXIe-1095 is calibrated during the manufacturing process and should be recalibrated annually to remove frequency error that accumulates over time (such as crystal aging). Refer to the ***PXIe-1095 Calibration Procedure*** at `ni.com/calibration` for more details.

You also can route the OCXO as the 10 MHz output reference to support systems with tight synchronization requirements.

10 MHz Input Reference

Several options are available to synchronize the system to an external clock:

- Drive a clock from an external source through the PXI_CLK10_IN pin on the System Timing Slot.
- Drive a clock from an external source through the 10 MHz REF IN SMA on the rear of the chassis (Timing and Synchronization upgrade only).
- Connect a high-density trigger cable from the Trig Port 1/10 MHz Ref Out port of another chassis to the Trig Port 0/10 MHz REF IN port of this chassis (Timing and Synchronization upgrade only).

When an external clock is detected on any of these inputs, the backplane automatically phase-locks the PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 signals to this external clock and distributes these signals to the slots. Refer to the ***PXIe-1095 Specifications*** for the specification information for an external clock provided on the PXI_CLK10_IN pin of the system timing slot or rear panel SMA.

If an external clock is present on more than one of these inputs, the signal is selected according to the following table.

Table 4. Backplane External Clock Input Truth Table

System Timing Slot PXI_CLK10_10	Rear 10 MHz REF IN SMA Connector	Trig Port 0/ 10 MHz REF IN Port	Backplane PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100
10 MHz clock present	—	—	Phase-locked to System Timing Slot PXI_CLK10_IN
No clock present	10 MHz clock present	—	Phase-locked to Rear 10 MHz REF IN SMA
No clock present	No clock present	10 MHz clock present	Phase-locked to Trig Port 0/ 10 MHz REF IN Port
No clock present	No clock present	No clock present	Backplane generates its own clocks. If the chassis has the Timing and Synchronization upgrade, the clocks are phase-locked to the OCXO.

10 MHz Output Reference

By default, a copy of the backplane's PXI_CLK10 is exported to the 10 MHz REF OUT SMA connector as well as the Trig Port 1/10 MHz REF OUT port on the rear of the chassis. Independent buffers drive these clocks. Refer to the ***PXIe-1095 Specifications*** for the rear SMA connector 10 MHz REF OUT signal specification information. This feature is available only with the Timing and Synchronization upgrade.

On a chassis with an OCXO, you also can select the OCXO as the source for the 10 MHz REF OUT signals. One application where this is useful is when you want multiple chassis to share the same timebase and have the same phase offset. In this application, select a chassis with an OCXO to be the master timebase for the system. On this master chassis, select the OCXO as the source for the 10 MHz REF OUT port. Connect the master chassis 10 MHz REF OUT port to a clock splitter, then route the clock to each chassis' 10 MHz REF IN port (including back to the master chassis). If you use matched-length cables, each chassis in the system is nominally matched in phase.

PXIe-1095 Installation

The following topics provide information on installing and connecting the PXIe-1095 chassis.

Unpacking

Carefully inspect the shipping container and the chassis for damage. Check for visible damage to the metal work. Check to make sure all handles, hardware, and switches are undamaged. Inspect the inner chassis for any possible damage, debris, or detached components. If the chassis was damaged during shipment, file a claim with the carrier. Retain the packing material for possible inspection and/or reshipment.

What You Need to Get Started

The PXIe-1095 chassis kit contains the following items:

- PXIe-1095 chassis
- Filler panel
- Software with ***PXI Platform Services 17.3*** or newer
- Chassis number labels

Note You also will need an AC power cable, sold separately. Refer to the following table for more information about AC power cables.

Table 5. AC Power Cables

Power Cable	Reference Standards
Standard 120 V (USA)	ANSI C73.11/NEMA 5-15-P
Switzerland 220 V	SEV 6534-2
Australia 240 V	AS C112
Universal Euro 230 V	CEE (7), II, IV, VII
United Kingdom 230 V	BS 1363

Power Cable	Reference Standards
Japan 100 V	JIS 8303

If you are missing any of the items or have the incorrect AC power cable, contact NI.

Safety Information

Caution Before undertaking any troubleshooting, maintenance, or exploratory procedure, carefully read the following caution notices.

Caution Protection may be impaired if equipment is not used in the manner specified.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

- Protective Earth—The facility installation must provide a means for connection to protective earth.
- Modification—Do not modify any part of the chassis from its original condition. Unsuitable modifications may result in safety hazards.

Warning High leakage current present when operating dual power supplies at 400 Hz to 440 Hz. When operating dual power supplies within this range, connect the chassis to earth ground before connecting to AC power.

- Protective Earth Terminal Wiring—Qualified personnel must install a protective earthing conductor from the chassis protective earth terminal (using an #8-32 SEMS screw) on the rear to the protective earth wire in the facility.

Grounding wire	2.1 mm^2 (14 AWG)
Ring lug	#8
Protective earth terminal torque	1.13 N · m (10 lb · in.)

- Chassis Grounding—The chassis requires a connection from the premise wire safety ground to the chassis ground. The earth safety ground must be connected during use of this equipment to minimize shock hazards. Refer to the ***Connecting Safety Ground*** section for instructions on connecting safety ground.
- Live Circuits—Operating personnel and service personnel must not remove protective covers when operating or servicing the chassis. Adjustments and service to internal components must be undertaken by qualified service technicians. During service of this product, the mains connector to the premise wiring must be disconnected. Dangerous voltages may be present under certain conditions; use extreme caution.
- Explosive Atmosphere—Do ***not*** operate the chassis in conditions where flammable gases are present. Under such conditions, this equipment is unsafe and may ignite the gases or gas fumes.
- Part Replacement—Only service this equipment with parts that are exact replacements, both electrically and mechanically. Contact NI for replacement part information. Installation of parts with those that are not direct replacements may cause harm to personnel operating the chassis. Furthermore, damage or fire may occur if replacement parts are unsuitable.

Chassis Cooling Considerations

The PXIe-1095 chassis is designed to operate on a bench or in an instrument rack. You must adhere to the cooling clearances as outlined in the following section.
Related reference:

- Providing Adequate Clearance
- Chassis Ambient Temperature Definition
- Installing Filler Panels
- Installing Slot Blockers

Providing Adequate Clearance

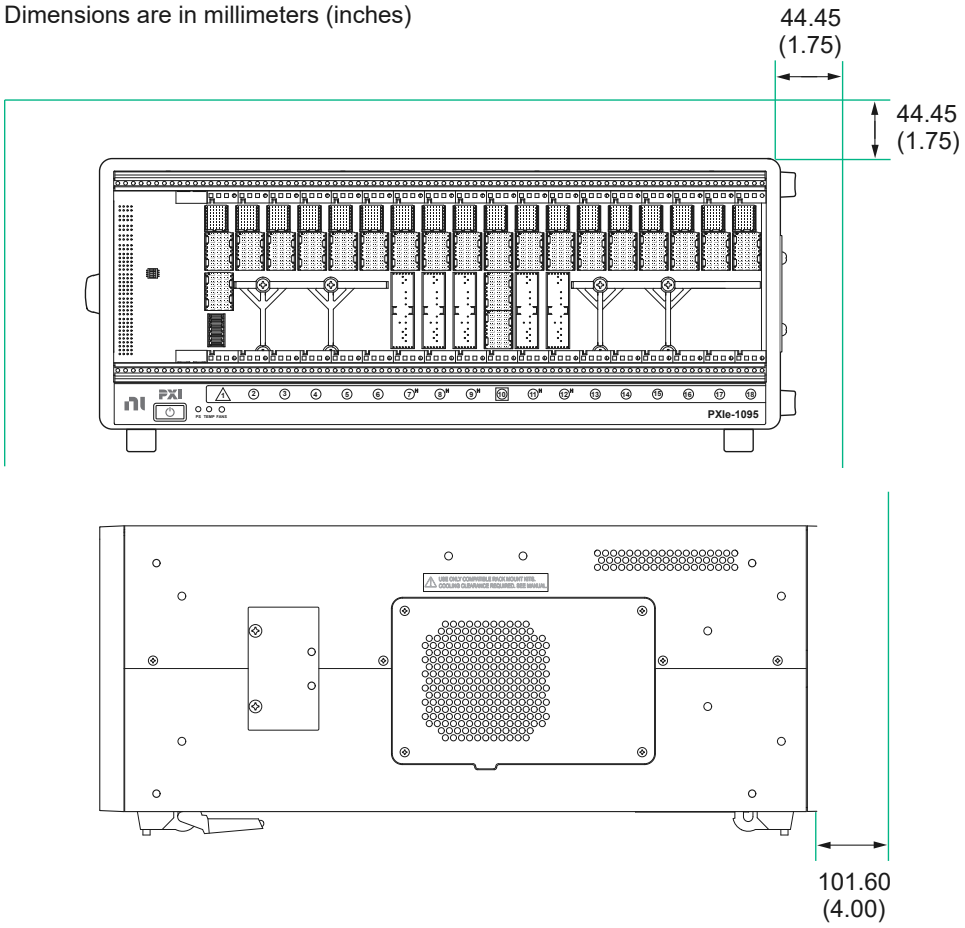
The module and power supply exhaust vents for the PXIe-1095 are on the top of the chassis. The module intake vents are on the rear of the chassis. There are also intake and exhaust vents located along the sides of the chassis.

Adequate clearance between the chassis and surrounding equipment, heat generating

devices, and air flow blockages must be maintained to ensure proper cooling. Minimum cooling clearances are shown in the following figure. For rack mount applications adequate forced air ventilation is required. For benchtop applications additional cooling clearances may be required for optimal air flow and reduced hot air recirculation to the air inlet fans.

Figure 11. PXIe-1095 Cooling Clearances

Dimensions are in millimeters (inches)



Caution Failure to provide these clearances may result in undesired thermal-related issues with the chassis or modules.

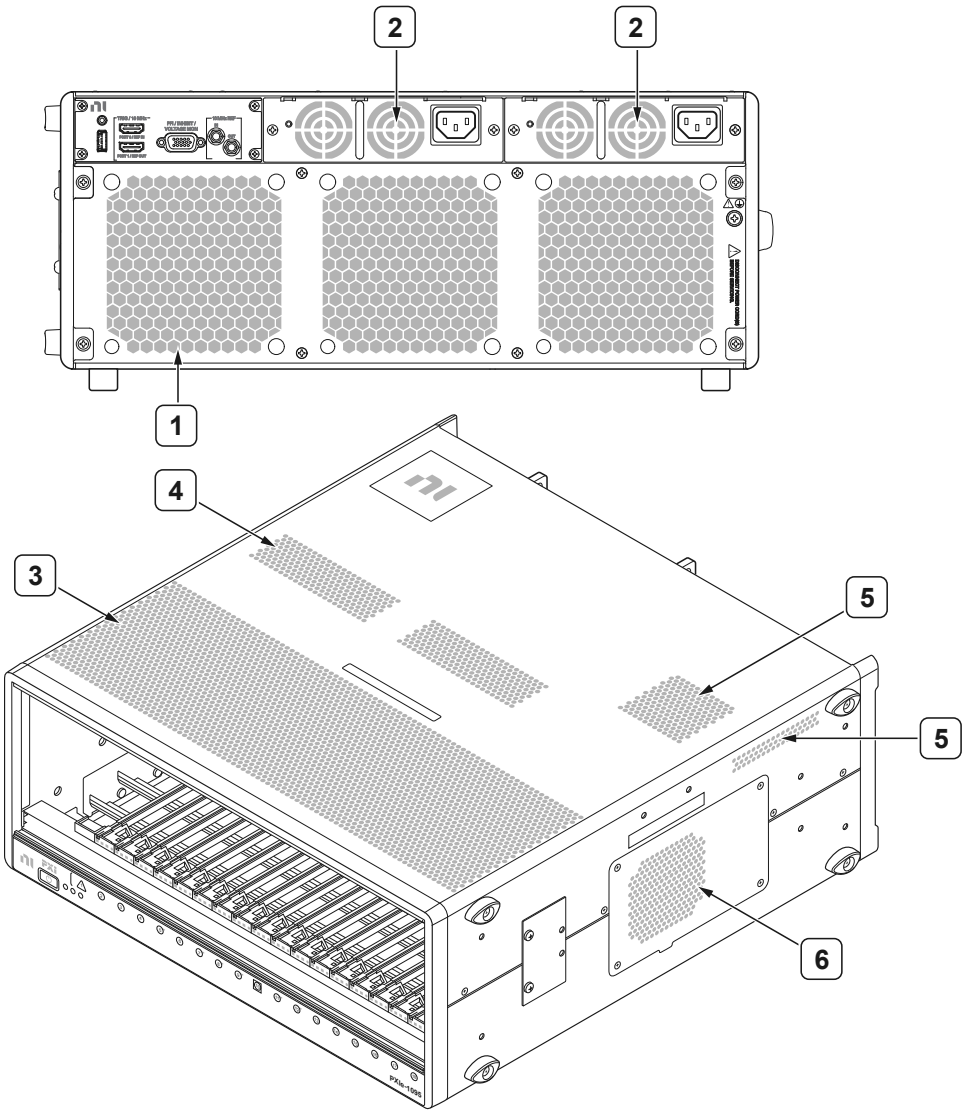
To aid in thermal health monitoring for either rack or benchtop use you can monitor the chassis intake temperatures in Measurement & Automation Explorer (MAX) to ensure the temperatures do not exceed the ratings in the ***Operating Environment*** section of the ***PXIe-1095 Specifications***.

Additionally, many PXI modules provide temperature values you can monitor to ensure

critical temperatures are not exceeded. Increasing chassis clearances, ventilation, reducing external ambient temperatures, and removing nearby heat sources are all options for improving overall chassis thermal performance.

The vent locations are shown in the following figure.

Figure 12. PXIe-1095 Vents



1. PXI Module Air Intake (3x)
2. Power Supply Intake (2x)
3. PXI Module Air Exhaust Vent
4. Power Supply Air Exhaust Vent (2x)
5. Timing and Synchronization Upgrade Air Exhaust Vent (2x)
6. Side Air Intake Vent (Right)/Side Air Exhaust Vent (Left)

Note The side exhaust vent (not shown) is located on the left side of the chassis.

Chassis Ambient Temperature Definition

The chassis fan control system uses ambient intake air temperatures for controlling fan speeds when in Auto mode. These temperatures may be higher than ambient room temperature depending on surrounding equipment and/or airflow blockages. Ensure ambient intake temperatures do not exceed the ratings in the ***Operating Environment*** section of the ***PXIe-1095 Specifications***. You can monitor the module ambient intake temperatures in NI Measurement & Automation Explorer (MAX).

Installing Filler Panels

To maintain proper module cooling performance, install filler panels (one is provided with the chassis) in unused or empty slots. Secure with the captive mounting screws provided.

Installing Slot Blockers

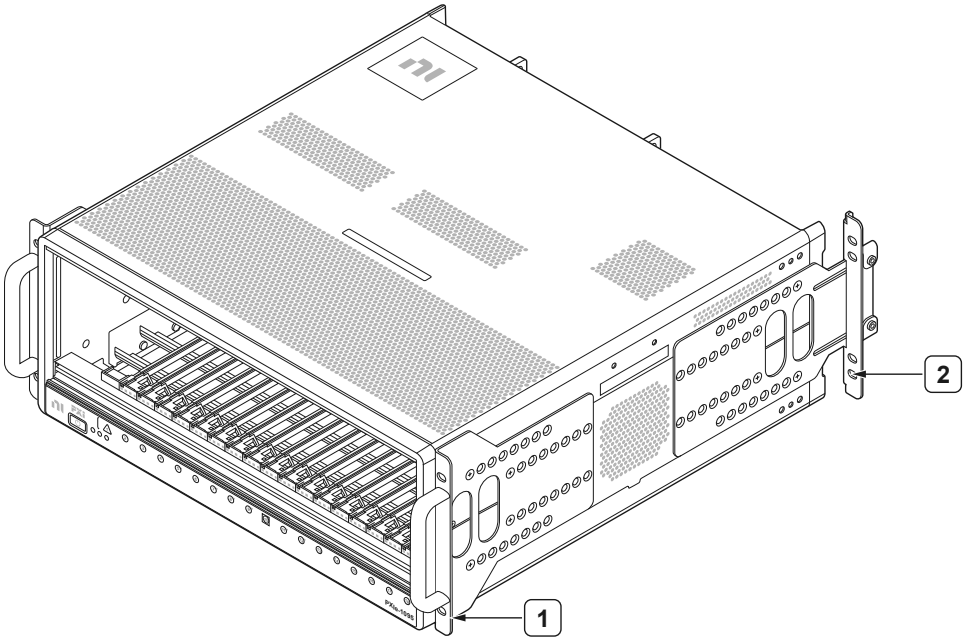
You can improve the cooling performance of the chassis by installing optional slot blockers. Refer to the NI website at ni.com/r/pxiblocker for more information about slot blockers.

Rack Mounting

Rack mount applications require optional rack mount kits available from NI. Refer to the instructions supplied with the rack mount kits to install your PXIe-1095 chassis in an instrument rack.

Note You must remove the feet and carry handle from the PXIe-1095 chassis when rack mounting.

Figure 13. PXIe-1095 Rack Mount Kit Components



1. Front Rack Mount (NI part number 786371-01)
2. Rear Rack Mount (NI part number 786372-01)

The front rack mount kit and rear rack mount kit each include both a long bracket and a short bracket to accommodate various rack depths.

Connecting the Safety Ground

Caution The PXIe-1095 chassis are designed with a three-position IEC 60320 C14 inlet for the U.S. that connects the ground line to the chassis ground. For proper grounding, a suitable cordset must be used to connect this inlet to an appropriate earth safety ground.

If your power outlet does not have an appropriate ground connection, you must connect the premise safety ground to the chassis grounding screw located on the rear panel. To connect the safety ground, complete the following steps:

1. Connect a 2.1 mm^2 (14 AWG) grounding wire to the chassis grounding screw (#8-32 SEMS) using an M4 grounding ring lug. The wire must have green insulation with a yellow stripe or must be noninsulated (bare).
2. Attach the opposite end of the wire to permanent earth ground using toothed

washers or a toothed lug tightened to 1.13 N · m (10 lb · in.) using an appropriate torque wrench or torque screwdriver.

Connecting to a Power Source

Caution Do not install modules prior to performing the following power-on test. To completely remove power, you must disconnect the AC power cable.

Attach input power through the rear AC inlet using the appropriate AC power cable supplied.

The Power Inhibit switch allows you to power on the chassis or place it in standby mode. With an empty chassis in Default Mode, press down the Power Inhibit switch and hold it down for four seconds. Observe that all fans become operational and all three front panel LEDs are a steady green. Pressing and holding the Power Inhibit switch again for four seconds will return the chassis to standby.

PXIe-1095 Configuration

The following topics provide information on preparing and operating the PXIe-1095 chassis.

Inhibit Mode

The PXIe-1095 chassis supports operation in two inhibit modes. Default mode is used when normal power inhibit button functionality is desired. In Default mode, when a system controller is installed in slot 1 of the chassis, the user can press the power inhibit button to power on the chassis.

Note In Default mode, you can also power on the chassis without a system controller installed in slot 1. To power on the chassis from standby, press and hold the power inhibit button for 4 seconds. To power off the chassis, again press and hold the power inhibit button for 4 seconds.

Manual mode is used when you would like to manually control the inhibit state of the chassis. In Manual mode, driving the Remote Inhibit signal high or floating it will cause the chassis to be powered on. Driving the Remote Inhibit signal low or shorting it to ground will cause main power to be inhibited.

Note The Timing and Synchronization upgrade is required for access to the Remote Inhibit signal. Without this upgrade, a chassis in Manual mode will always be powered on when AC power is connected.

Related reference:

- Inhibit Mode Selection

Inhibit Mode Selection

You can select the chassis Inhibit Mode using Measurement & Automation Explorer (MAX). Refer to the ***Inhibit Mode Configuration in MAX*** section for more

information.

You also can select the chassis Inhibit Mode on the PXIe-1095 chassis using a DIP switch on the backplane. Refer to the ***DIP Switches*** section for more information about DIP switch settings. Refer to Front View of the PXIe-1095 for the switch location.

Note The DIP switch must be in the Default position for software configuration in MAX to work. If the DIP switch is in the Manual position, the Inhibit Mode will be Manual regardless of the software setting.

Related reference:

- Chassis Components
- DIP Switches
- Inhibit Mode Configuration in MAX

Fan Mode

The PXIe-1095 chassis operates in two main fan modes.

In Auto mode, the chassis intake air temperature determines the chassis fans' speed. Select Auto mode for improved acoustic performance.

In High mode, the chassis fans' speed is fixed at high speed regardless of chassis intake air temperature. Select High mode for maximum cooling performance.

Related reference:

- Cooling Profiles
- Fan Mode Selection

Cooling Profiles

Both fan modes are available within the 38 W and 58 W/82 W cooling profiles.

- 38 W cooling profile supports NI modules up to 38 W max power dissipation
- 58 W cooling profile supports NI modules up to 58 W max power dissipation from

0 °C to 55 °C.
- 82 W cooling profile supports NI modules up to 82 W max power dissipation from 0 °C to 40 °C.

Note PXI Platform Services software includes services to optimize acoustics while meeting cooling requirements. In some cases, lower cooling profiles may be disabled because they are inadequate for the modules in the chassis.

Note Only the listed fan operation modes are supported. Contact NI if you have questions regarding a specific application.

Fan Mode Selection

The chassis fan mode can be selected using Measurement & Automation Explorer (MAX). Refer to the ***Fan Configuration in MAX*** section for more information.

Alternatively, the fan mode on the PXIe-1095 chassis is selected using a DIP switch on the backplane. Refer to the ***DIP Switches*** section for more information about the DIP switch.

Note The DIP switch must be in the Auto position for software configuration in MAX to work. If the DIP switch is in the High position, the chassis fan mode will be High regardless of the software setting.

Related tasks:

- Fan Configuration in MAX

Related reference:

- DIP Switches

PXI_CLK10 Rear Panel Connectors

With the Timing and Synchronization upgrade, there are two SMA connectors on the

rear of the chassis for PXI_CLK10. The connectors are labeled 10 MHz REF IN and OUT. You can use them for supplying the backplane with PXI_CLK10 or routing the backplane's PXI_CLK10 to another chassis. Refer to the ***System Reference Clock*** section for details about these signals.

High-Density Triggers

With the Timing and Synchronization upgrade, the PXIe-1095 supports routing PXI triggers between chassis using a pair of high-density trigger connectors on the rear of the chassis.

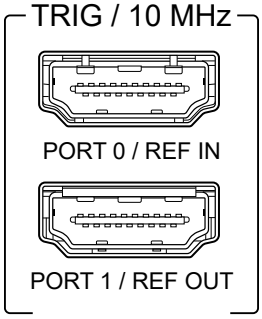
The following table shows the high-density trigger connector pinout.

Table 6. High-Density Trigger Connector Pinout

Pin	Signal Top Port	Signal Bottom Port
1	Trig(0)	
2	Logic Ground	
3	Trig(4)	
4	Trig(1)	
5	Logic Ground	
6	Trig(5)	
7	Trig(2)	
8	Logic Ground	
9	Trig(6)	
10	10 MHz Ref In +	10 MHz Ref Out +
11	Logic Ground	
12	10 MHz Ref In -	10 MHz Ref Out -
13	Reserved	
14	Trig(3)	
15	SCL	
16	SDA	

Pin	Signal Top Port	Signal Bottom Port
17	Logic Ground	
18	Presence Detect	
19	Trig(7)	

Figure 14. High-Density Trigger Ports



Routing triggers between chassis requires using a NI API such as NI-DAQmx. You can target the individual pins of each trigger port as sources or destinations for PXI triggers to or from a PXI module. If the chassis are connected to the same host via MXI, targeting these pins is not necessary; you can specify a source device in one chassis and a destination device in another chassis, and the software makes the necessary trigger routes automatically.

Notice The high-density trigger ports are not HDMI interfaces. Do not connect the high-density trigger ports on the PXIe-1095 to the HDMI interface of another device. NI is not liable for any damage resulting from such signal connections.

Notice You can use off-the-shelf HDMI cables to connect adjacent chassis. However, because off-the-shelf cables may be of varying quality, for best performance use NI-recommended cables available at ni.com.

Notice For proper operation, you must cable the Port 1/Ref Out port of one chassis to Port 0/Ref In of the adjacent chassis. Do not connect Port 0/Ref In to Port 0/Ref In of another chassis. Do not connect Port 1/Ref Out to Port 1/Ref Out of another chassis. While no damage will occur in either of these

configurations, the trigger routing capabilities will not be functional.

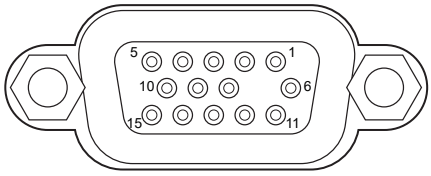
Note You can route triggers either direction out of either trigger port.

Remote Inhibit and Chassis Monitoring

With the Timing and Synchronization upgrade, the PXIe-1095 chassis supports remote voltage monitoring and inhibiting through a female 15-pin connector on the rear panel. The following table shows the 15-pin connector pinout.

Table 7. Remote Inhibit and Chassis Monitoring Connector Pinout

Pin	Signal
1	Logic Ground
2	+5 V
3	Fault (Active High)
4	+3.3 V
5	Inhibit (Active Low)
6	+12 V
7	Key
8	-12 V
9	Logic Ground
10	PFI3
11	PFI2
12	Logic Ground
13	PFI1
14	PFI0
15	Logic Ground

Pin	Signal
	

You can use a digital voltmeter to ensure all chassis voltage levels are within the allowable limits. Referring to the previous table, connect one voltmeter lead to a supply pin on the 15-pin remote voltage monitoring connector on the rear panel. Connect the voltmeter reference lead to one of the ground pins. Compare each voltage reading to the values in the following table.

Caution When connecting digital voltmeter probes to the rear 15-pin connector, be careful not to short the probe leads together.

Note Use the rear-panel 15-pin connector only to check voltages. Do not use the connector to supply power to external devices.

Table 8. Power Supply Voltages at Chassis Monitoring Connector

Pin	Supply	Acceptable Voltage Range
2	+5 V	4.75 V to 5.25 V
4	+3.3 V	3.135 V to 3.465 V
6	+12 V	11.4 V to 12.6 V
8	-12 V	-12.6 V to -11.4 V
1, 9, 12, 15	Logic Ground	0 V

If the voltages fall within the specified ranges, the chassis complies with the CompactPCI voltage-limit specifications.

You can use the Inhibit signal to control the chassis inhibit state manually when the inhibit mode is set to Manual. Refer to the ***Inhibit Mode*** section for more

information. Refer to the ***PXIe-1095 Specifications*** for the Inhibit signal input requirements.

The Fault signal indicates when a fault condition is detected on the chassis. The signal definition is shown in the following table. Refer to the ***PXIe-1095 Specifications*** for the Fault signal voltage specifications.

Table 9. Fault Signal Definition

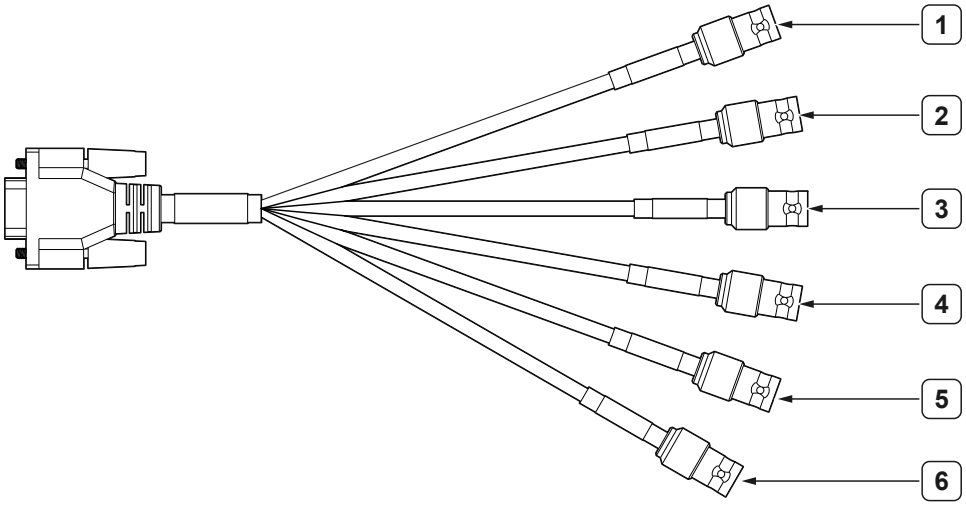
State	Description
Low	Chassis is operating normally
High	An abnormal operating condition has been detected

Examples of abnormal operating conditions include but are not limited to: intake or exhaust temperature outside of chassis operating range, a chassis fan has failed, or a chassis voltage is outside its specified operating range.

You can use the four Programmable Function Interface (PFI) lines to route triggers to/from PXI modules in the chassis. Routing triggers to the PFI lines requires using an NI API such as NI-DAQmx. You can target the individual PFI lines as sources or destinations for PXI triggers to or from a PXI module. Refer to the ***PXIe-1095 Specifications*** for the PFI line input and output specifications.

Note An optional DSUB-to-BNC cable (NI Part Number 149055-0R2) that interfaces with the remote inhibit and chassis monitoring port is available from NI. The cable enables use of the inhibit, fault, and PFI 0-3 lines through BNC.

Figure 15. Optional DSUB-to-BNC Cable



1. Fault (Active High)
2. Inhibit (Active Low)
3. PFI 0
4. PFI 1
5. PFI 2
6. PFI 3

USB Port

With the Timing and Synchronization upgrade, the PXIe-1095 has a single USB 3.0 Type A port on the rear of the chassis. The following table lists and describes the USB 3.0 connector signals.

Table 10. USB 3.0 Connector Signals

Pin	Signal Name	Signal Description
1	VBUS	Cable Power (+5 V)
2	Data-	USB Data–
3	Data+	USB Data+
4	GND	Ground
5	StdA_SSRX–	USB Data Receive–
6	StdA_SSRX	USB Data Receive+
7	GND DRAIN	Ground

Pin	Signal Name	Signal Description
8	StdA_SSTX–	USB Data Transmit–
9	StdA_SSTX+	USB Data Transmit+

The PXIe-1095 chassis uses a Texas Instruments TUSB7340 USB 3.0 Host Controller as the interface for the rear USB port.

Note Drivers for this device are required for Windows 7 and are available for download at `www.ti.com/lit/zip/sllc423`.

PXI Express System Configuration with MAX

The PXI Platform Services software included with your chassis automatically identifies your PXI Express system components to generate a `pxiesys.ini` file. You can configure your entire PXI system and identify PXI-1 chassis through Measurement & Automation Explorer (MAX), included with your system controller. PXI Platform Services creates the `pxiesys.ini` and `pxisys.ini` file, which define your PXI system parameters.

Note The configuration steps for single or multiple-chassis systems are the same.

MAX provides the following chassis information:

- Asset information, such as serial number or part number
- Chassis number
- Voltages, temperatures, and fan speed
- Fan and cooling settings
- Slot details
- Chassis self-test
- Firmware update

Note Information available through MAX may vary based on your chassis

> variant or firmware and platform services version.

Related tasks:

- Trigger Configuration in MAX
- PXI Trigger Bus Routing
- Fan Configuration in MAX

Related reference:

- Inhibit Mode Configuration in MAX

Trigger Configuration in MAX

PXI Platform Services provides an interface to route and reserve triggers so dynamic routing, through drivers such as DAQmx, avoids double-driving and potentially damaging trigger lines. For more information about routing and reserving PXI triggers, refer to ni.com/r/pxitiming.

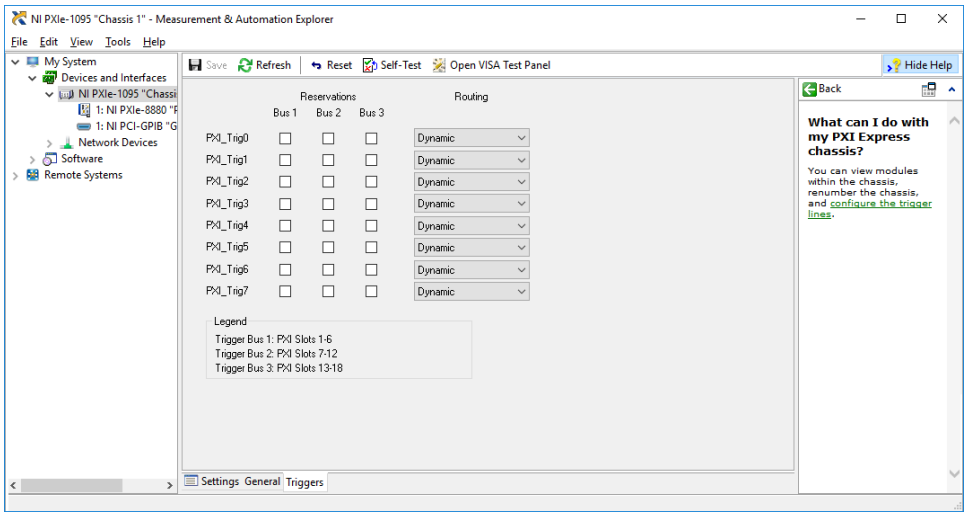
Each chassis has one or more trigger buses, each with eight lines numbered 0 through 7 that can be reserved and routed statically or dynamically. Static reservation ***pre-allocates*** a trigger line to prevent its configuration by a user program. Dynamic reservation/routing/deallocation is ***on the fly*** within a user program based on NI APIs such as NI-DAQmx. NI recommends dynamic reservations and routing are used whenever possible. If static reservations are required, static reservation of trigger lines can be implemented by the user in MAX through the Triggers tab. PXI modules dynamically configured by programs such as NI-DAQmx will not use reserved trigger lines. This prevents the instruments from double-driving the trigger lines, possibly damaging devices in the chassis. In the default configuration, trigger lines on each bus are independent. For example, if trigger line 3 is asserted on trigger bus 0, by default it is not asserted automatically on any other trigger bus.

Complete the following steps to reserve these trigger lines in MAX.

1. In the Configuration tree, click the PXI chassis branch to configure.
2. In the lower right pane, click the Triggers tab.
3. Select the trigger lines to statically reserve.

4. Click the Save button.

Figure 16. Trigger Configuration in MAX



PXI Trigger Bus Routing

Some NI chassis, such as the PXIe-1095, have the capability to route triggers from one bus to others within the same chassis using the **Trigger Routing** tab in MAX.

> **Note** Selecting any non-disabled routing automatically reserves the line in all trigger buses being routed to. If you are using NI-DAQmx, it will reserve and route trigger lines for you, so you won't have to route trigger lines manually.

Complete the following steps to configure trigger routings in MAX.

1. In the **Configuration** tree, select the chassis in which you want to route trigger lines.
2. In the right-hand pane, select the **Trigger Routing** tab near the bottom.
3. For each trigger line, select **Away from Bus 1**, **Away from Bus 2**, or **Away from Bus 3** to route triggers on that line in the described direction, or select **Dynamic** for the default behavior with no manual routing.
4. Click the **Save** button.

Inhibit Mode Configuration in MAX

You can configure inhibit mode behavior using software settings in MAX. The PXIe-1095

supports both Default and Manual inhibit modes. Refer to the ***Inhibit Mode*** section for more information about these modes.

Complete the following steps to change the chassis inhibit mode in MAX:

1. In the Configuration tree, select the PXI chassis you want to configure.
2. In the right-hand pane, click the Settings tab.
3. In the Power Supplies group, select the desired Inhibit Mode using the drop-down menus.
4. Click the Save button.

Related reference:

- Inhibit Mode

Fan Configuration in MAX

You can configure fan behavior using software settings in MAX.

The PXIe-1095 supports both Auto and High fan modes for both the 38 W and 58 W cooling profiles. Refer to the ***Fan Mode*** section for more information about these modes.

You may also select a Manual fan mode. In this mode, you may manually set the fan speeds to achieve the desired performance.

Note You may not set the fan speeds or power settings lower than the minimum level required to maintain required cooling levels.

Complete the following steps to change the fan settings in MAX .

1. In the Configuration tree, click on the PXI chassis you want to configure.
2. In the right-hand pane, click on the Settings tab.
3. In the Fans group, select the desired Mode and Cooling Profile using the drop-down menus.
4. Click the Save button. Shortly after clicking the Save button, you should see the fan speeds change.

Related reference:

- Fan Mode Selection

Using System Configuration and Initialization Files

The PXI Express specification allows many combinations of PXI Express chassis and system modules. To assist system integrators, the manufacturers of PXI Express chassis and system modules must document the capabilities of their products. The minimum documentation requirements are contained in `.ini` files, which consist of ASCII text. System integrators, configuration utilities, and device drivers can use these `.ini` files.

The capability documentation for the PXIe-1095 chassis is contained in the `chassis.ini` file on the software media that comes with the chassis. The information in this file is combined with information about the system controller to create a single system initialization file called `pxisys.ini` (PXI System Initialization). The system controller manufacturer either provides a `pxisys.ini` file for the particular chassis model that contains the system controller or provides a utility that can read an arbitrary `chassis.ini` file and generate the corresponding `pxisys.ini` file. System controllers from NI provide the `pxisys.ini` file for the PXIe-1095 chassis, so you should not need to use the `chassis.ini` file. Refer to the documentation provided with the system controller or to ni.com/support for more information on `pxisys.ini` and `chassis.ini` files.

Device drivers and other utility software read the `pxisys.ini` file to obtain system information. The device drivers should have no need to directly read the `chassis.ini` file. For detailed information regarding initialization files, refer to the PXI Express specification at `www.pxisa.org`.

Maintenance

Enter a short description of your reference here (optional).

This section describes basic maintenance procedures you can perform on the PXIe-1095 chassis.

Caution Disconnect the power cable prior to servicing your PXIe-1095 chassis.

Service Interval

Clean dust from the chassis exterior (and interior) as needed, based on the operating environment. Periodic cleaning increases reliability.

Preparation

The information in this section is designed for use by qualified service personnel. Read the ***Read Me First: Safety and Electromagnetic Compatibility*** document included with your kit before attempting any procedures in this section.

Note Many components within the chassis are susceptible to static discharge damage. Service the chassis only in a static-free environment. Observe standard handling precautions for static-sensitive devices while servicing the chassis. ***Always*** wear a grounded wrist strap or equivalent while servicing the chassis.

Cleaning

Cleaning procedures consist of exterior and interior cleaning of the chassis and cleaning the fan filters. Refer to your module's user documentation for information about cleaning individual CompactPCI or PXI Express modules.

Caution Always disconnect the power cable prior to servicing the chassis.

Interior Cleaning

Use a dry, low-velocity stream of air to clean the interior of the chassis. Use a soft-bristle brush for cleaning around components.

Exterior Cleaning

Clean the exterior surfaces of the chassis with a dry, lint-free cloth or a soft-bristle brush. If any dirt remains, wipe with a cloth moistened in a mild soap solution. Remove any soap residue by wiping with a cloth moistened with clear water. Do not use abrasive compounds on any part of the chassis.

Caution Avoid getting moisture inside the chassis during exterior cleaning, especially through the top vents. Use just enough moisture to dampen the cloth.

Do not wash the front- or rear-panel connectors or switches. Cover these components while cleaning the chassis.

Do not use harsh chemical cleaning agents; they may damage the chassis. Avoid chemicals that contain benzene, toluene, xylene, acetone, or similar solvents.

Replacing the Power Supply

This section describes how to remove, configure, and install the AC power supply in the PXIe-1095 chassis.

Caution Disconnect the power cable prior to replacing the power supply.

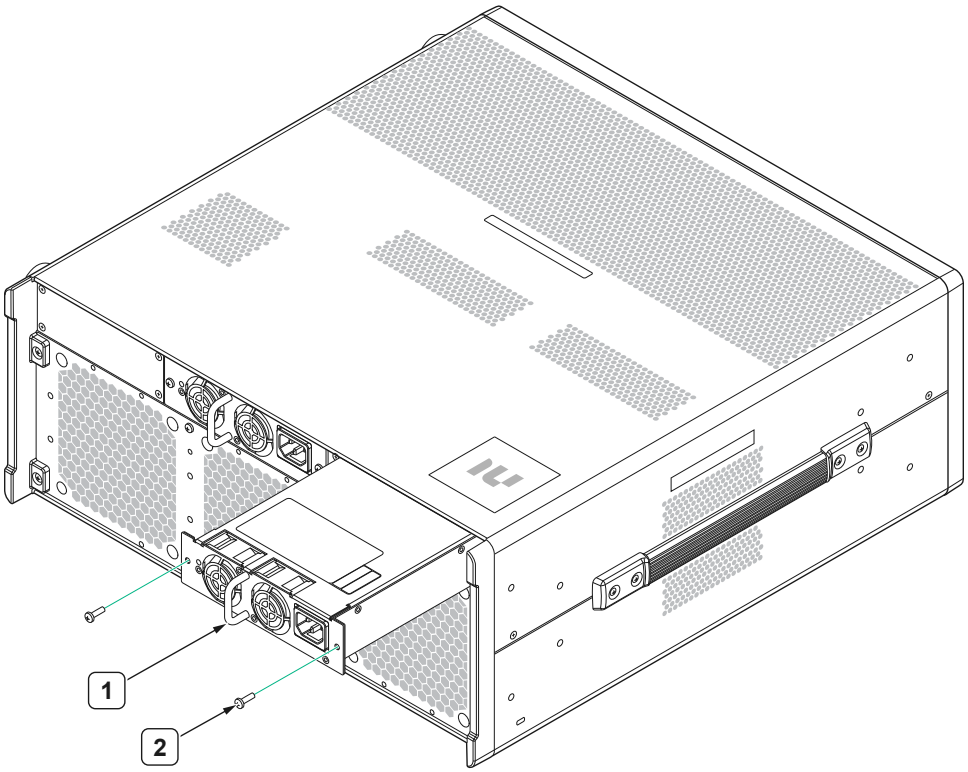
Before connecting the power supply shuttle to a power source, read this section and

the ***Read Me First: Safety and Electromagnetic Compatibility*** document included with the kit.

Removal

The PXIe-1095 power supply is a replacement part for the PXIe-1095 chassis. Before attempting to replace the power supply, verify there is adequate clearance behind the chassis. Disconnect the power cables from the power supplies on the back of the chassis, or, if operating in redundant mode and you wish to replace a single supply, disconnect only the power cable to the supply being replaced. If operating in redundant power mode, wait at least 30 seconds for the supply's internal power to dissipate. Identify the two mounting screws for the PXIe-1095 that attach the power supply to the chassis. Refer to the following figure for the screw locations. Using a Phillips screwdriver, remove the screws. Pull on the two rear handles of the power supply to remove it from the back of the chassis.

Figure 17. Removing the Power Supply



1. Power Supply
2. Power Supply Screws (2x)

Installation

Note The power supply should be disconnected from AC power for at least 30 seconds before it is installed in the chassis.

Ensure that there is no visible damage to the new power supply. Verify that the housing and connector on the new power supply assembly have no foreign material inside. Install the new power supply into the chassis in the reverse order of removal. Replace and tighten two #6-32 screws with a Phillips screwdriver. Connect the AC inlet power cable.

To meet the Shock and Vibration specifications listed in the ***PXIe-1095 Specifications***, tighten screws to 1.3 N · m (11.5 in · lb) of torque.

Connecting the Safety Ground

Caution The PXIe-1095 chassis are designed with a three-position IEC 60320 C14 inlet for the U.S. that connects the ground line to the chassis ground. For proper grounding, a suitable cordset must be used to connect this inlet to an appropriate earth safety ground.

If your power outlet does not have an appropriate ground connection, you must connect the premise safety ground to the chassis grounding screw located on the rear panel. To connect the safety ground, complete the following steps:

1. Connect a 2.1 mm^2 (14 AWG) grounding wire to the chassis grounding screw (#8-32 SEMS) using an M4 grounding ring lug. The wire must have green insulation with a yellow stripe or must be noninsulated (bare).
2. Attach the opposite end of the wire to permanent earth ground using toothed washers or a toothed lug tightened to 1.13 N · m (10 lb · in.) using an appropriate torque wrench or torque screwdriver.

Connecting to a Power Source

Caution Do not install modules prior to performing the following power-on test. To completely remove power, you must disconnect the AC power cable.

Attach input power through the rear AC inlet using the appropriate AC power cable supplied.

The Power Inhibit switch allows you to power on the chassis or place it in standby mode. With an empty chassis in Default Mode, press down the Power Inhibit switch and hold it down for four seconds. Observe that all fans become operational and all three front panel LEDs are a steady green. Pressing and holding the Power Inhibit switch again for four seconds will return the chassis to standby.

Installing Replacement Fan Assemblies

This section describes how to remove and install the fan assemblies in a PXIe-1095 chassis.

Caution Disconnect all power cables and wait at least 30 seconds prior to replacing fan assemblies.

Replacing the PXI Module Fan Assembly

Before attempting to replace the rear module fan assembly, verify that there is adequate clearance behind the chassis. Disconnect all power cables from the power supplies on the back of the chassis. Wait at least 30 seconds for the supplies' internal power to dissipate.

Follow these steps to remove the fan assembly:

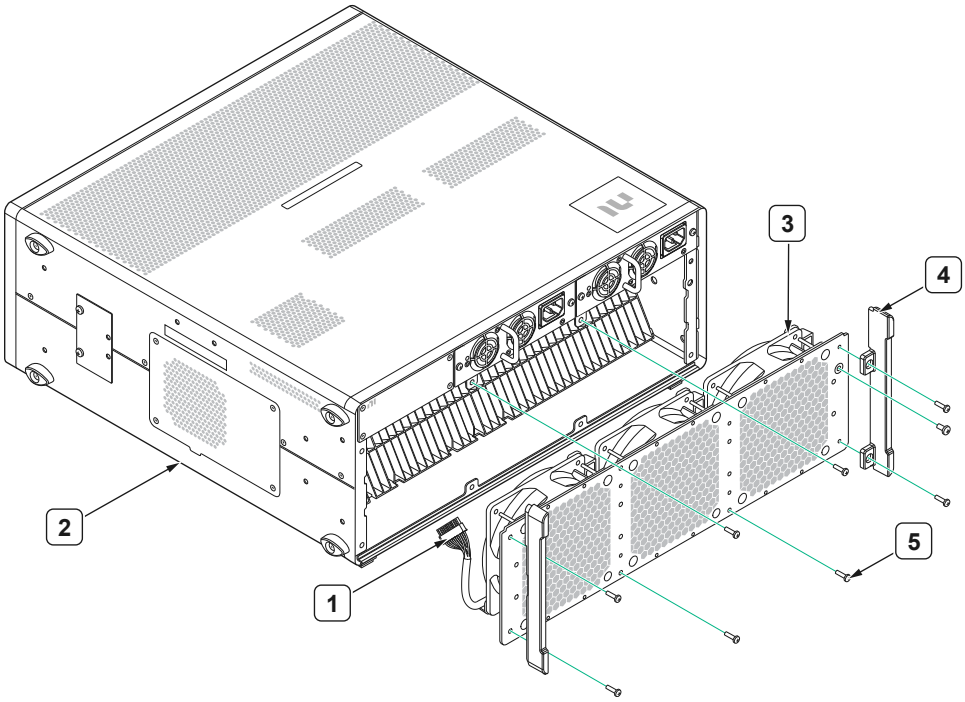
1. Using a Phillips screwdriver, remove the eight #6-32 mounting screws and #8-32 ground screw that attach the fan panel to the chassis. Refer to the ***Replacing Rear Fan Module*** figure below for more details.
2. Remove the rear chassis feet.

3. With the internal fan harness still connected, carefully pull and rotate the fan assembly from the rear cavity of the chassis. Use caution when removing the fan assembly to avoid damaging the fan wire harness.
4. Disconnect the fan harness from the internal chassis receptacle as shown in the ***Replacing Rear Fan Module*** figure.

Follow these steps to install a new fan assembly:

1. Angle the fan assembly to install the fan harness plug into the internal chassis receptacle. Use care to avoid damaging the fan harness or receptacle.
2. Connect the internal fan harness and install the fan assembly into the rear cavity of the chassis as shown in the ***Internal Fan Harness*** figure. Use caution when installing the fan panel assembly to avoid pinching or damaging the wire harness.
3. Replace the chassis feet.
4. Using a Phillips screwdriver, tighten the eight #6-32 mounting screws and #8-32 ground screw into the rear of the chassis. To meet the shock and vibration specifications listed in the ***PXIe-1095 Specifications***, tighten the screws to 1.3 N · m (11.5 lb · in.) of torque.

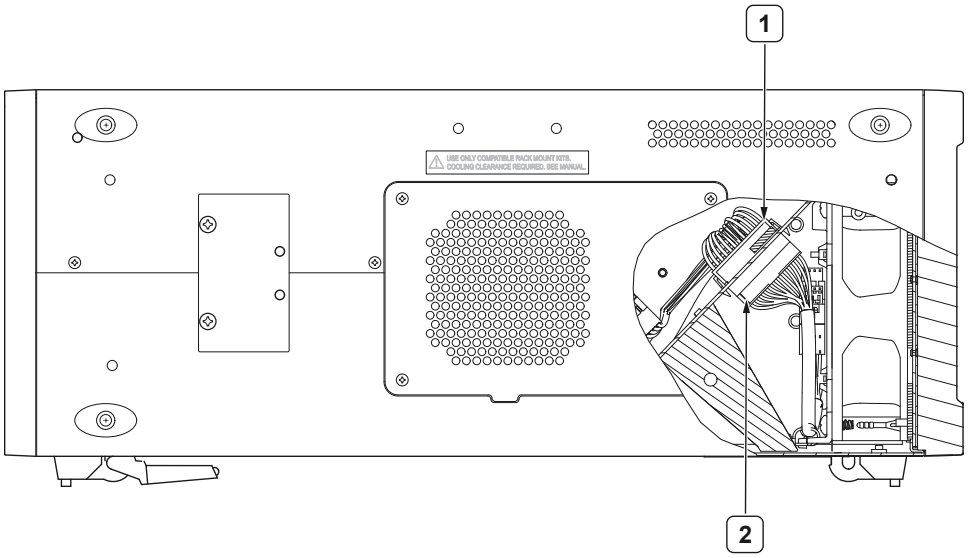
Figure 18. Replacing Rear Fan Module



1. Fan Harness Plug

2. PXIe-1095 Chassis
3. PXI Module Fan Assembly
4. Rear Chassis Feet (2x)
5. Mounting Screws (8x)

Figure 19. Internal Fan Harness



1. Fan Receptacle
2. Fan Harness Plug

Replacing the Side Fan Assembly

Before attempting to replace the side fan assembly, verify that there is adequate clearance to the side of the chassis. Disconnect all power cables from the power supplies on the back of the chassis. Wait at least 30 seconds for the power supplies' internal power to dissipate.

Complete the following steps to remove the side fan assembly:

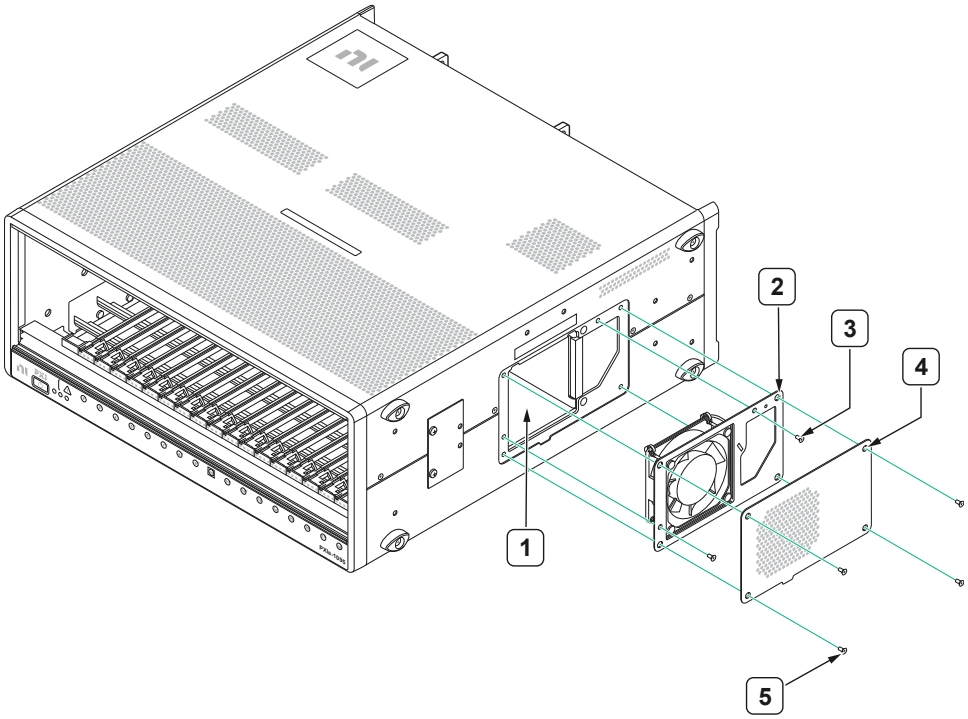
1. Using a Phillips screwdriver, remove the four #4-40 mounting screws that attach the side fan cover, as shown in the ***Replacing the Side Fan Assembly*** figure below.
2. Remove the side fan cover from the chassis.
3. Using a Phillips screwdriver, remove the two #2-56 mounting screws that hold the side fan assembly to the chassis.

4. Locate the side fan assembly harness in the internal chassis cavity and disconnect the fan from the chassis receptacle. Use caution when removing the fan assembly to avoid damaging the internal wire harness.
5. Pull the side fan assembly straight from the chassis and remove it.

Complete the following steps to install a new side fan assembly:

1. Plug the side fan assembly plug into the internal chassis fan receptacle.
2. Set the side fan assembly into the chassis side fan cavity. Use caution when placing the wire harness into the chassis to avoid damaging the internal or fan wire harness.
3. Using a Phillips screwdriver, hand tighten the two #2-56 side assembly mounting screws. Use the side fan cutout to pull clear extra cable from the chassis side panels to prevent pinching. To meet the shock and vibration specifications in the ***PXIe-1095 Specifications***, tighten the screws to 0.6 N · m (5.0 lb · in.) of torque.
4. Place all the extra cable into the chassis side fan cavity.
5. Using a Phillips screwdriver, tighten the four #4-40 side fan cover mounting screws to the chassis. To meet the shock and vibration specifications in the ***PXIe-1095 Specifications***, tighten the screws to 0.8 N · m (6.7 lb · in.) of torque.

Figure 20. Replacing the Side Fan Assembly



1. Chassis Side Fan Cavity
2. Side Fan Assembly
3. Side Fan Retention Bracket Mounting Screws (2x)
4. Side Fan Cover
5. Side Fan Cover Mounting Screws (4x)

Calibration

The following section applies to PXIe-1095 chassis with the Timing and Synchronization upgrade.

The PXIe-1095 chassis is factory calibrated before shipment at approximately 25 °C to the levels indicated in the ***PXIe-1095 Specifications***. The associated calibration constant is stored in the onboard nonvolatile memory.

The factory calibration of the PXIe-1095 involves calculating and storing one calibration constant that sets the OCXO frequency. The OCXO that the PXIe-1095 uses features electronic frequency control. This allows fine-tuning the OCXO by varying the control voltage to the OCXO. The chassis uses a 16-bit digital-to-analog converter (DAC) to give precise control of the tuning voltage. A single calibration constant sets the DAC value. This constant is adjusted during factory calibration to meet the specification listed in the ***PXIe-1095 Specifications***.

Refer to `ni.com/calibration` for additional information about NI calibration services.