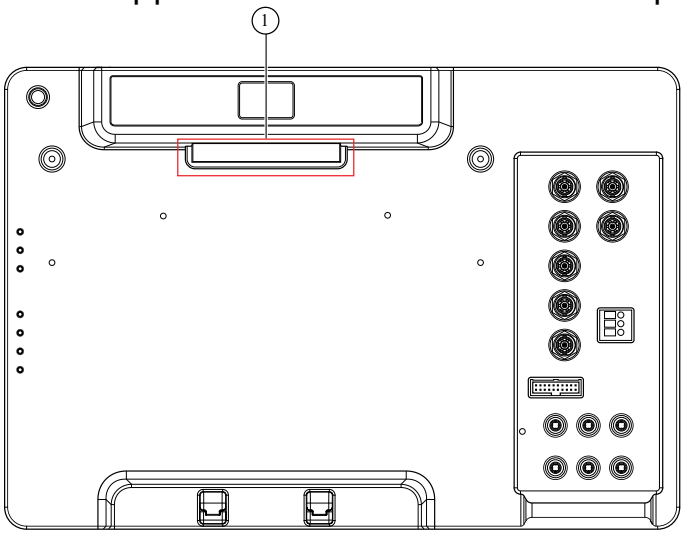
NI ELVIS III Using Your Control I/O

2025-03-20

Contents

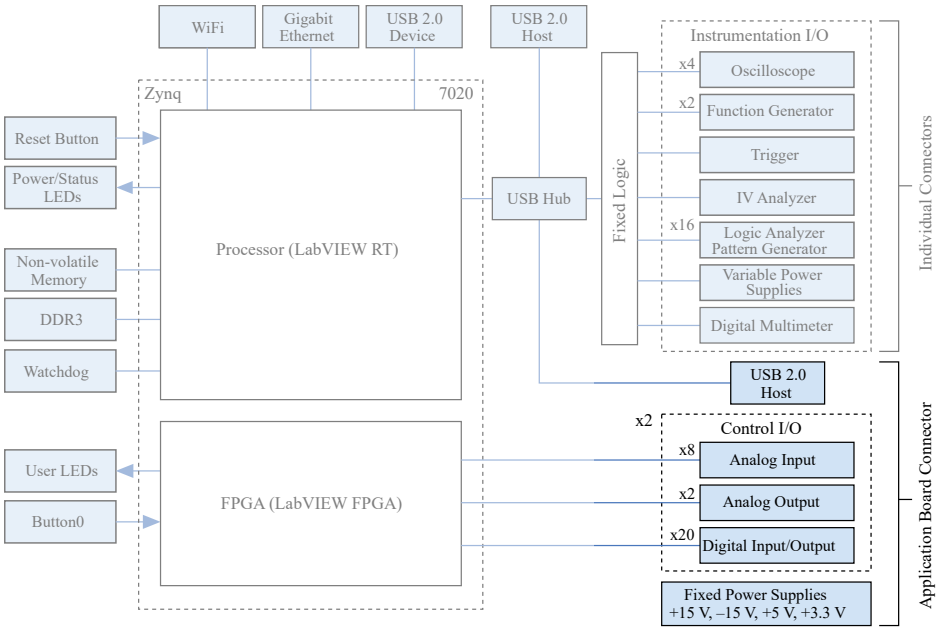
Using the Control I/O

The control I/O consists of analog input, analog output, digital input/output, and fixed power supplies. These resources are internally controlled by the FPGA, and can be programmatically accessed from LabVIEW FPGA and LabVIEW RT. The control I/O is provided by the NI ELVIS III on the application board connector. When you insert an application board, these resources are directly connected to the application board. Not all application boards will utilize or expose all of these resources.



1. Application board connector

The following diagram shows the NI ELVIS III hardware architecture with the control I/O highlighted.



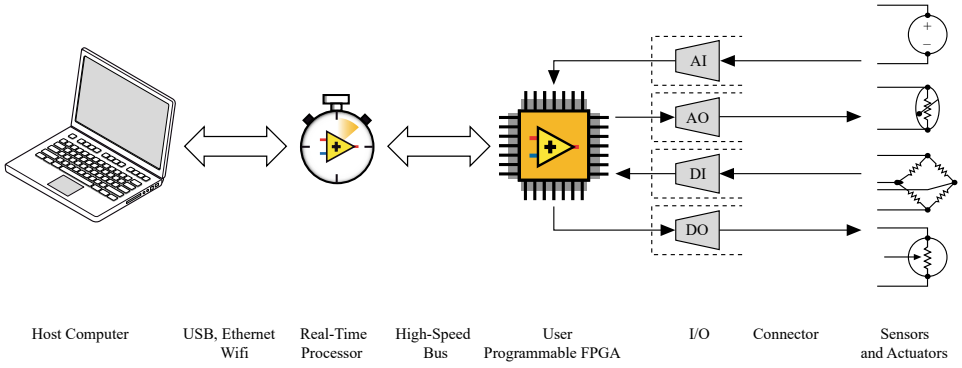
The NI ELVIS III Prototyping Board that is included in the NI ELVIS III kit exposes all of the control I/O through solderless breadboard strips located on either side of the central build area. Signals are grouped by function, and are individually labeled on each solderless breadboard strip. Refer to the NI ELVIS III Prototyping Board section for more information on the prototyping board.

Programming the Control I/O

The control I/O is part of the LabVIEW RIO architecture, which combines the LabVIEW Real-Time (RT) system, a user programmable FPGA, and user programmable I/O.

Find the control I/O, also known as user programmable I/O in the following diagram.

Figure 2. NI ELVIS III RIO Architecture



The NI ELVIS III provides three levels of programming that give you access to the control I/O:

- LabVIEW RT Express VIs
- LabVIEW RT Low Level VIs
- LabVIEW FPGA I/O nodes

Refer to LabVIEW RIO Architecture for an introduction to the LabVIEW Real-Time system and LabVIEW FPGA.

LabVIEW RT Express VIs

The LabVIEW ELVIS III Toolkit includes configuration-based Express VIs to enable the rapid development of user programs.

These Express VIs simplify the creation of applications that fulfill common I/O operations, such as waveform acquisition and generation, PWM output, encoder input, SPI communication, and so on, by eliminating the need for users to program with the FPGA. When you create a LabVIEW RT application using the Express VIs, a predefined FPGA personality is automatically downloaded to the FPGA. This FPGA personality implements all of the low level functionality required to support the execution of the Express VIs on the RT processor.

The Express VIs support the following functionality:

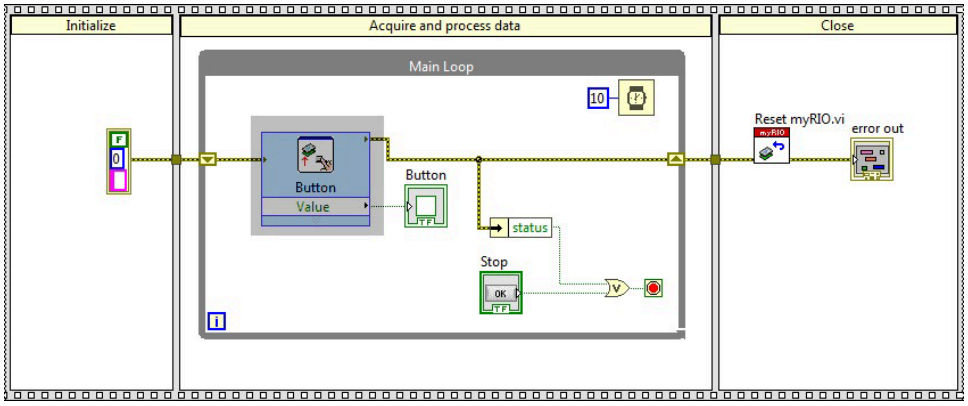
Function	Number of Channels
Analog Input (1 Sample)	16
Analog Input (n Samples)	16
Analog Input (continuous)	16
Analog Output (1 Sample)	4
Analog Output (n Samples)	4
Analog Output (continuous)	4
Digital Input (1 Sample)	40
Digital Input (n Samples)	40

Function	Number of Channels
Digital Output (1 Sample)	40
Digital Output (n Samples)	40
PWM Output	40
Encoder Input	20
SPI	2
I2C	2
UART	2
Interrupt	8
Button	1
LED	4

One sample, n samples, and continuous are three I/O modes of signal acquisition and generation. Continuous mode is available only for analog signals. For Express VIs that support different I/O modes, not all functions can operate simultaneously, due to resource conflicts. Refer to the LabVIEW ELVIS III Toolkit Help for more information about the I/O modes.

You cannot use an Express VI or Low Level VI in n samples mode to open channels from both banks. You can use two VIs in parallel and configure one to open channels from Bank A and another to open channels from Bank B.

The following figure shows an example of using the Button Express VI (highlighted) to acquire values from the user programmable button and display the values using a Boolean indicator. Refer to User Programmable Button for more details about the button. You can find this example in the LabVIEW Example Finder.

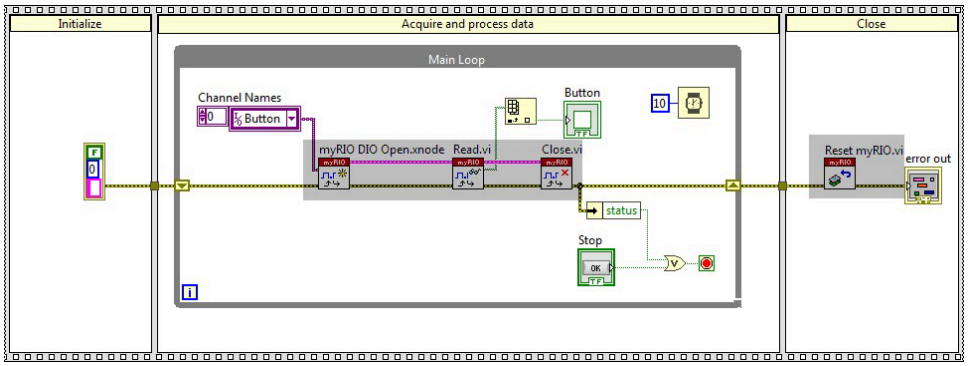


Refer to the LabVIEW ELVIS III Toolkit Help for more information about these Express VIs.

LabVIEW RT Low Level VIs

The LabVIEW ELVIS III Toolkit also includes Low Level VIs that provide fully programmatic access to the predefined FPGA personality. This gives you more flexibility in configuring each function, while retaining the ease of use of LabVIEW RT programming. The Low Level VIs provide very similar functionality as the Express VIs, but at a lower level of abstraction.

The following figure shows an example of using the Low Level VIs (highlighted) to open a reference to the user button, read the button value, and display the value by using a Boolean indicator.



Refer to the LabVIEW ELVIS III Toolkit Help for more information about these Low Level VIs.

LabVIEW FPGA I/O Nodes

The LabVIEW FPGA I/O nodes provide the lowest level of access to the control I/O and offer the highest degree of flexibility and performance.

Instead of using a predefined FPGA personality with fixed functionality, you can define your own functions by using the LabVIEW FPGA I/O nodes. LabVIEW FPGA allows for not only direct control of the control I/O, but also direct implementation of algorithms and data transfer in the FPGA. After defining the FPGA personality, you can then create a LabVIEW RT application that runs on the RT processor for high-level operations or further processing. You do not need to use an FPGA application in conjunction with an RT application.

The following figures show a LabVIEW FPGA application which reads values from the user button. The FPGA Main Default VI uses the FPGA I/O Node (highlighted) to write the values of the user button to the **DI.BTN** control. The RT Main VI uses the Read/Write Control method (highlighted) to read the value from the `DI.BTN` control and display it in the `Button Value` indicator.

Refer to Getting Started With LabVIEW FPGA for a series of videos that help you get started with building a LabVIEW FPGA application. Refer to the ***LabVIEW Help*** for more information about these FPGA I/O.

Figure 3. LabVIEW FPGA Project

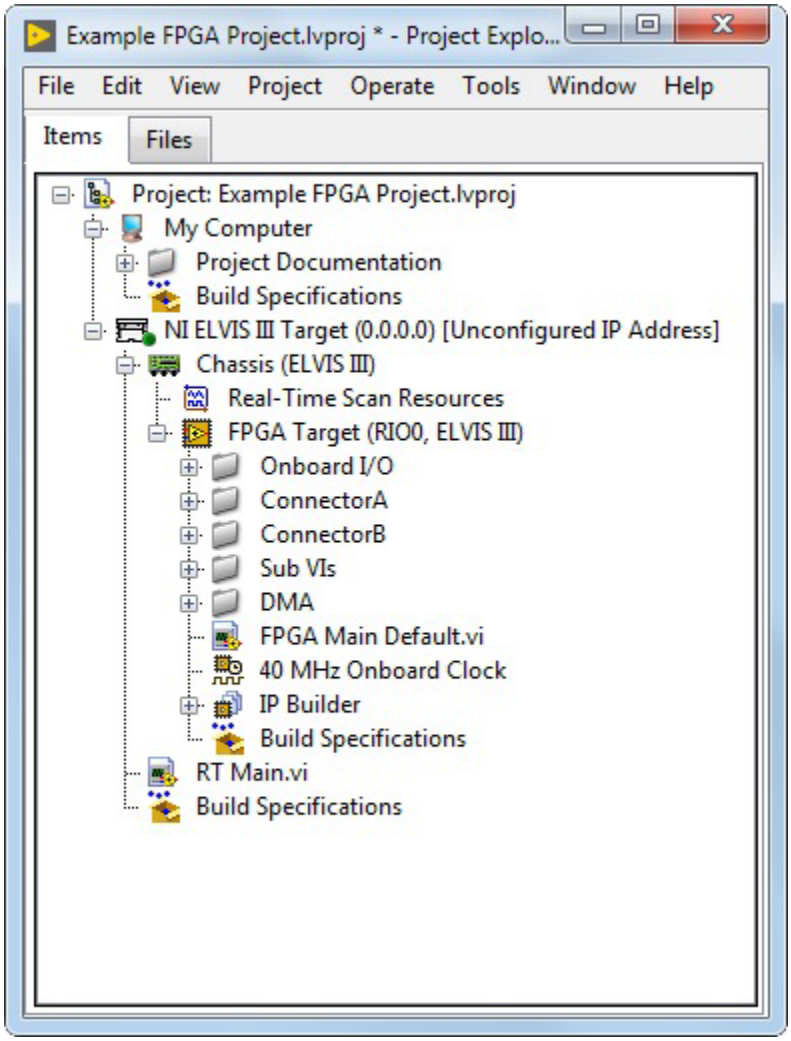


Figure 4. FPGA Main Default VI

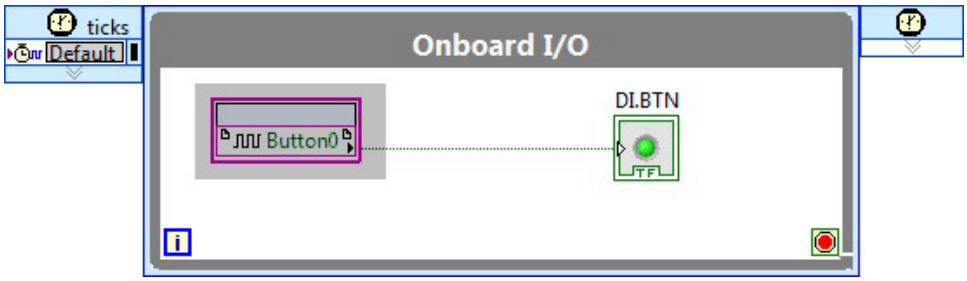
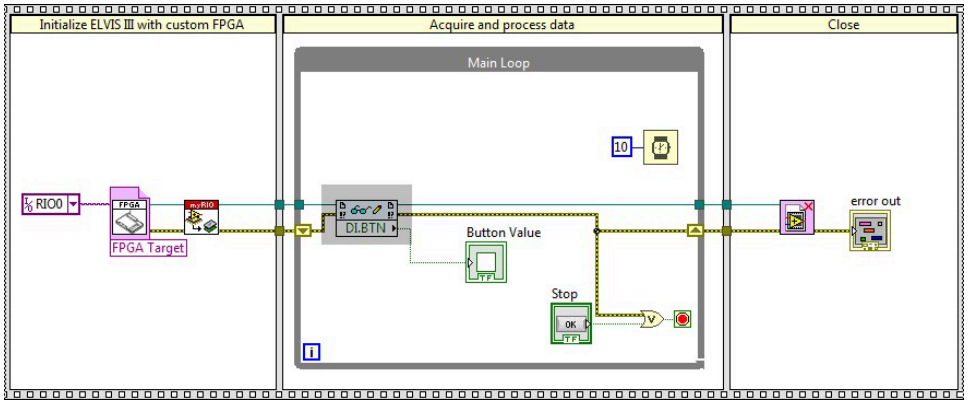


Figure 5. RT Main VI



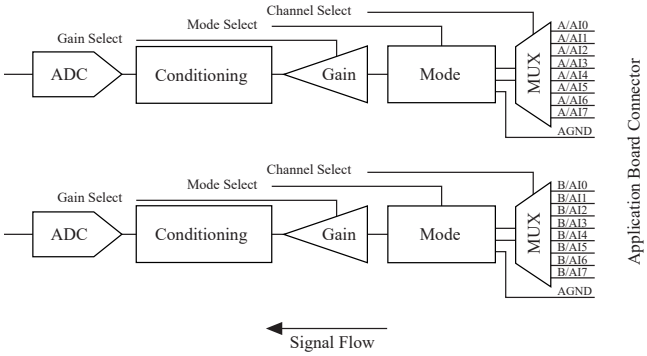
Related information:

- Getting Started with LabVIEW Real-Time Module
- Creating a Real-Time Application
- Getting Started with LabVIEW FPGA
- LabVIEW FPGA Help

Analog Input

The analog input section consists of two identical banks of analog inputs which are capable of operating independently of each other. Each bank includes an analog-to-digital converter (ADC), conditioning circuit, gain selector, mode selector, and channel multiplexer. The gain stage determines the input range for the conversion. The mode selection controls whether the input is configured for single-ended or differential measurement. The channel multiplexer selects the active channel(s) for the application.

Figure 6. Analog Input Circuitry



Connecting Signals to Analog Input

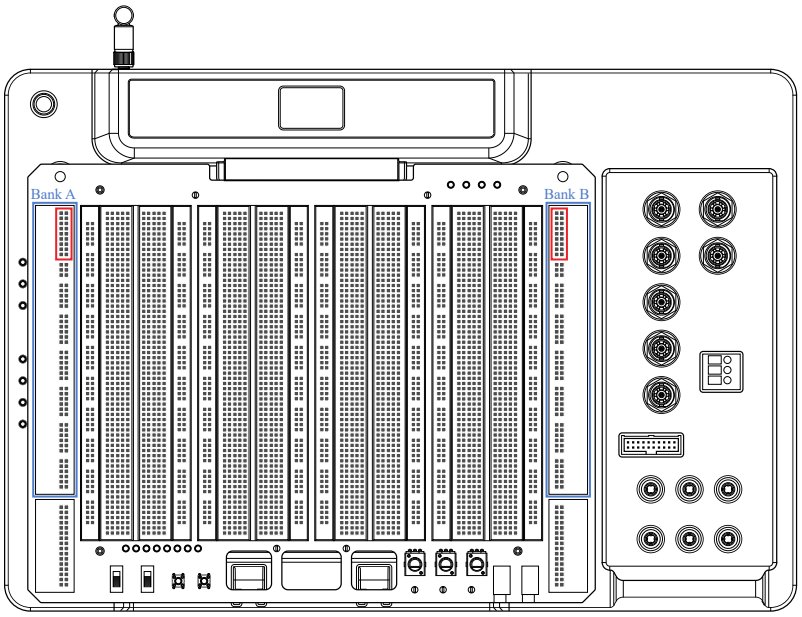
A single-ended measurement measures the difference between the selected signal and AI Ground. A differential measurement measures the difference between the selected signal and its associated signal pair. The following table shows the channel mapping for each mode.

Table 1. Analog Input Signal Mapping

Application Board Terminals		**Differential Mode (Default)**	**Single-ended Mode**
Bank A	A/AI0	AI 0 +	AI 0
	A/AI1	AI 1 +	AI 1
	A/AI2	AI 2 +	AI 2
	A/AI3	AI 3 +	AI 3
	A/AI4	AI 0 -	AI 4
	A/AI5	AI 1 -	AI 5
	A/AI6	AI 2 -	AI 6
	A/AI7	AI 3 -	AI 7
Bank B	B/AI0	AI 0 +	AI 0
	B/AI1	AI 1 +	AI 1
	B/AI2	AI 2 +	AI 2
	B/AI3	AI 3 +	AI 3
	B/AI4	AI 0 -	AI 4
	B/AI5	AI 1 -	AI 5
	B/AI6	AI 2 -	AI 6
	B/AI7	AI 3 -	AI 7
AGND		Analog Ground	Analog Ground

Notice Use AGND for analog signals only.

You can use the NI ELVIS III Prototyping Board to access these signals. The following diagram shows the NI ELVIS III with the analog input terminals highlighted.



To learn more about the Analog Input and grounding considerations, go to the Analog Input section in the Appendix.

Refer to the NI ELVIS III Prototyping Board section on how to access these signals on the NI ELVIS III prototyping board.

Programming Analog Input with LabVIEW

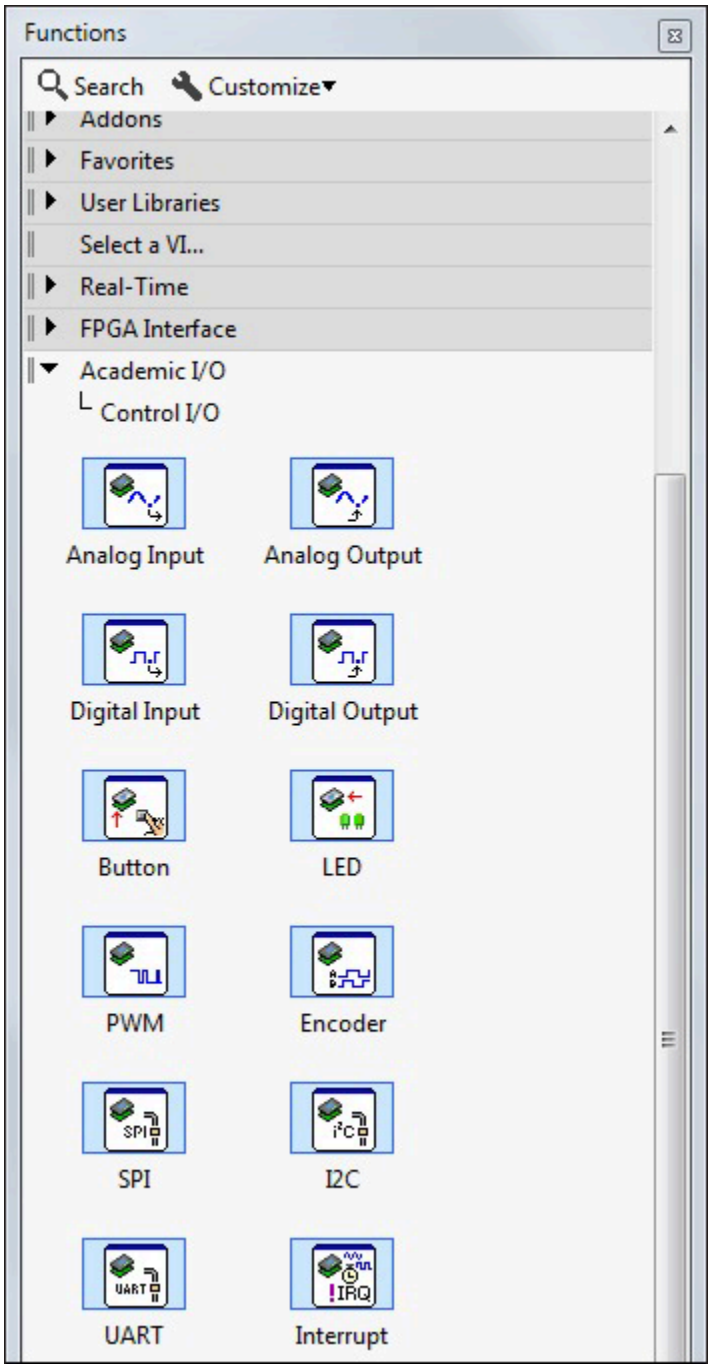
You can use LabVIEW Real-Time (RT) Express VIs, LabVIEW RT Low Level VIs, and LabVIEW FPGA I/O nodes to program the Analog Input channels.

Programming Examples

The LabVIEW ELVIS III Toolkit provides examples of using analog input channels to perform signal acquisition. You can find these examples in the `labview\examples\ELVIS III\Real-Time Control Applications\Analog IO\Analog IO.lvproj` directory.

LabVIEW RT Express VIs

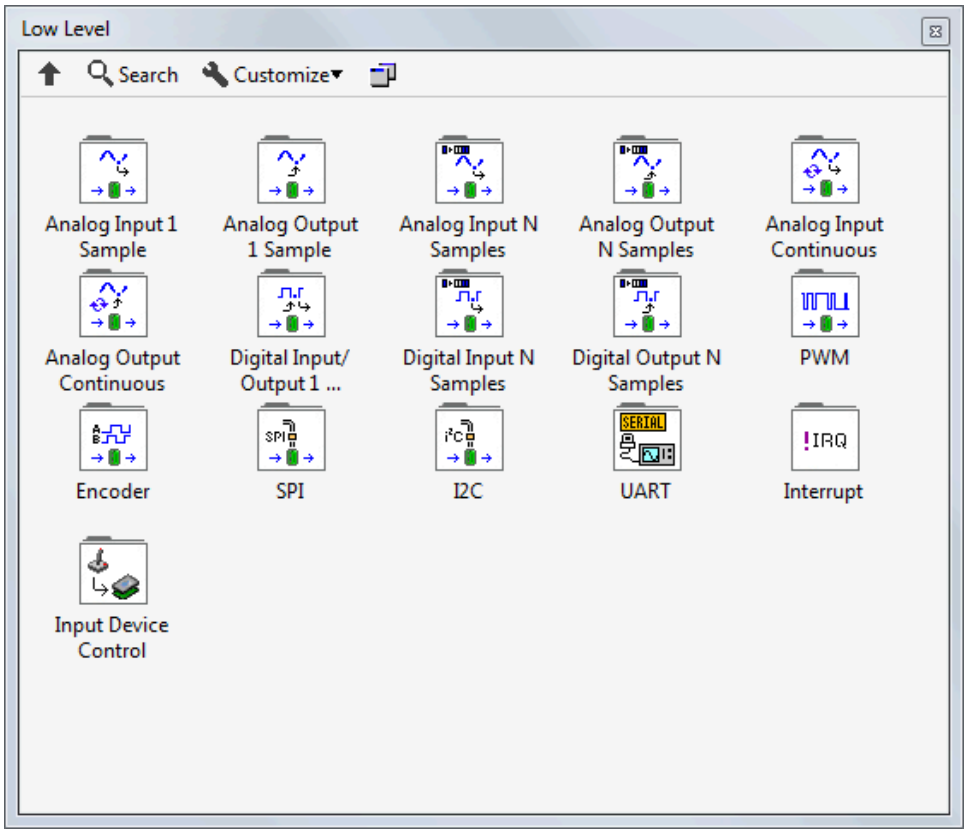
Use the Express VIs to interactively configure the settings for the I/O channels. When you place an Express VI on the block diagram or double-click an Express VI, a configuration dialog box appears. Use this configuration dialog box to configure the Express VI. Find the Express VIs on the **Academic I/O** » **Control I/O** subpalette on the Functions palette, as shown in the following figure:



The LabVIEW ELVIS III Toolkit provides Analog Input Express VI to access the Analog Input channels.

LabVIEW RT Low Level VIs

Use the Low Level VIs to have more programmatic access to settings of I/O channels. For example, you can use the Low Level VIs to open or close certain channels and change the channel configuration at run time. Find the Low Level VIs on the Low Level palette, as shown in the following figure:

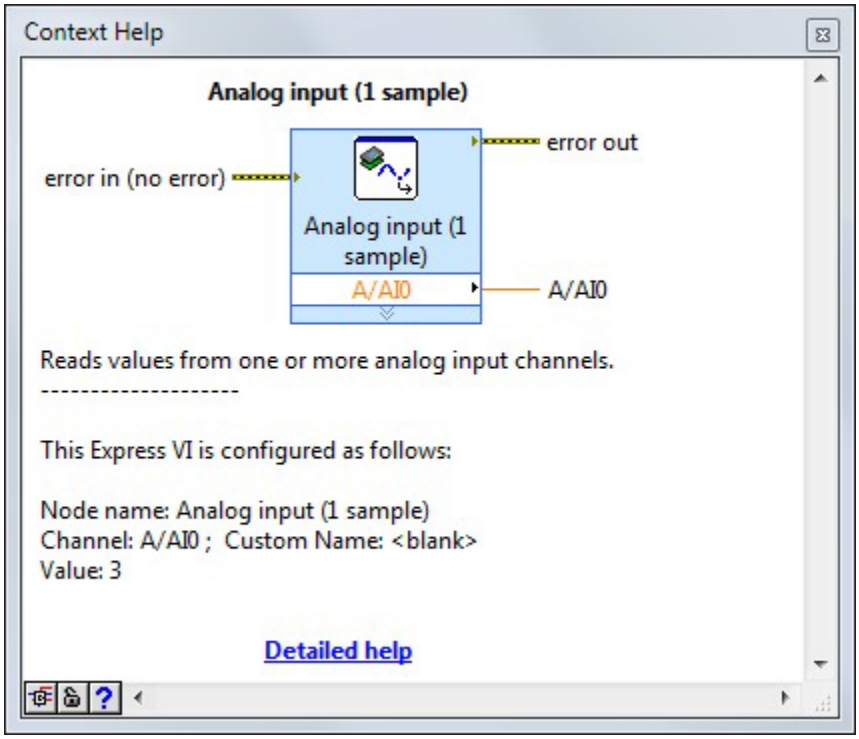


The LabVIEW ELVIS III Toolkit provides the following Low Level VIs to access the Analog Input channels:

- Analog Input 1 Sample VIs
- Analog Input N Samples VIs

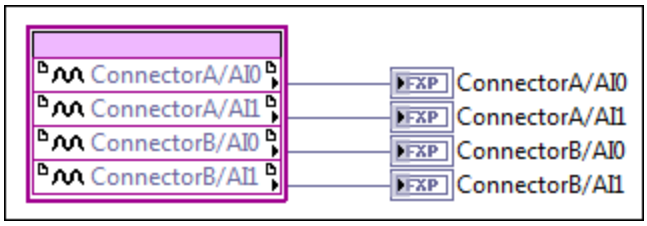
- Analog Input Continuous VIs

Select **Help » Show Context Help** or press <Ctrl-H> to display the Context Help window, from where you learn the basic information about each of the Express VIs and Low Level VIs. To learn more details about the VIs, refer to the ***LabVIEW ELVIS III Toolkit Help*** by clicking **Detailed help** at the bottom of the Context Help window, shown as follows:



LabVIEW FPGA I/O Nodes

Use the FPGA I/O nodes from the FPGA palette to access the Analog Input channels on the NI ELVIS III. You can also use the FPGA I/O property nodes if needed. Channels from both banks on the NI ELVIS III can be used in a single FPGA I/O node. The I/O banks are denoted as connectors in the software. The following figure shows a VI that uses FPGA I/O nodes to read inputs from AI channels 0 to 1 on Bank A and Bank B.



The FPGA palette does not provide any devoted FPGA I/O nodes for specific protocols such as PWM and Encoder. To access these protocols, use the LabVIEW RT VIs instead.

Refer to the **FPGA I/O Functions** section of the ***LabVIEW FPGA Module Help*** for detailed information about using the FPGA I/O nodes to perform operations on FPGA targets. Refer to the **NI ELVIS III** section in the ***NI Compact RIO Device Drivers Help*** to learn what terminals and I/O methods and properties you can access for the NI ELVIS III. You can access these help files by selecting **Help** » **LabVIEW Help** in LabVIEW, or search for their online versions on ni.com/manuals.

Analog Input Specifications

Specifications are ***Typical*** unless otherwise noted.

Number of banks	2, capable of independent operation
Number of channels per bank	8 single-ended or 4 differential
ADC resolution	16 bits
Input range	±10 V, ±5 V, ±2 V, ±1 V
Maximum sampling rate (single channel)	1 MS/s

Large signal bandwidth (-3 dB)	>500 kHz

Table 2. Analog Input Accuracy

Measurement Conditions	Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Typical (25 °C ± 5 °C)	0.064%	0.004%
Maximum (10 °C to 35 °C)	0.397%	0.054%

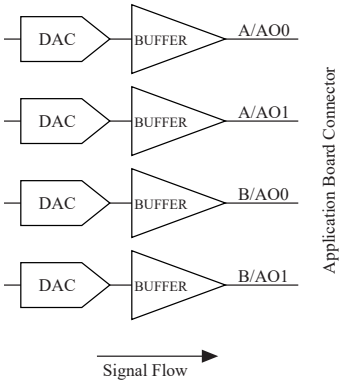
Recommended sampling rate (multi-channel)	≤500 kS/s aggregate
Multi-channel settling time	2 µs (±16 LSB for full scale step)
Input impedance	
Powered on	>1 GΩ
Powered off	>850 Ω
Overvoltage protection	
Powered on	±25 V, up to two AI lines
Powered off	±15 V, up to two AI lines

Analog Output

The analog output section consists of four identical channels of analog output. Each channel consists of a digital-to-analog converter (DAC) and output buffer with a fixed ±10 V output range. There are no hardware dependencies between the four channels,

and updates on one channel have no impact on the other channels. The channels can also be operated synchronously, providing simultaneous updates on any combination of the four channels.

Figure 7. Analog Output Circuitry



Connecting Signals to Analog Output

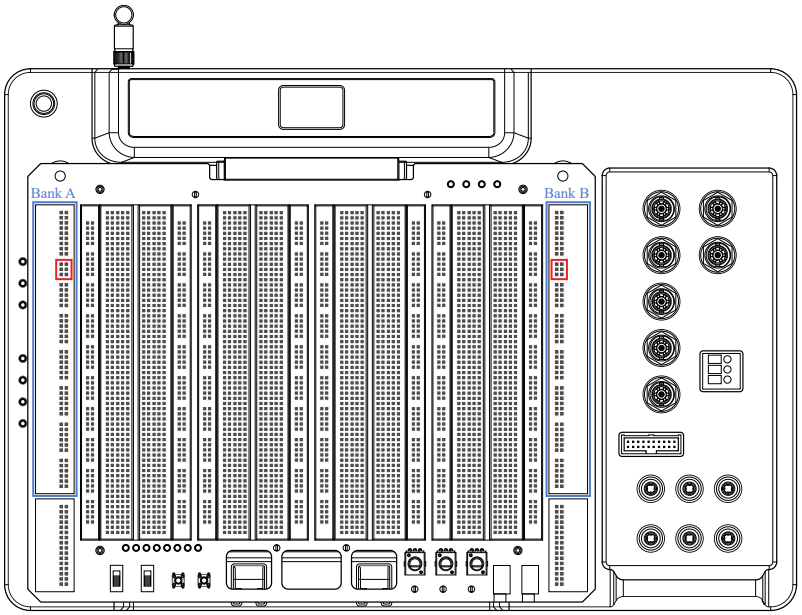
There are no configuration settings for the analog output channels. All of the analog output channels are single-ended. Each analog output is always referenced to the analog ground (AGND). The following table shows the channel mapping.

Table 3. Analog Output Signal Mapping

Application Board Terminals		**Signal**
Bank A	A/AO0	AO 0
	A/AO1	AO 1
Bank B	B/AO0	AO 0
	B/AO1	AO 1
AGND		Analog Ground

Notice Use AGND for analog signals only.

You can use the NI ELVIS III Prototyping Board to access these signals. The following diagram shows the NI ELVIS III with the analog output terminals highlighted.



Programming Analog Output with LabVIEW

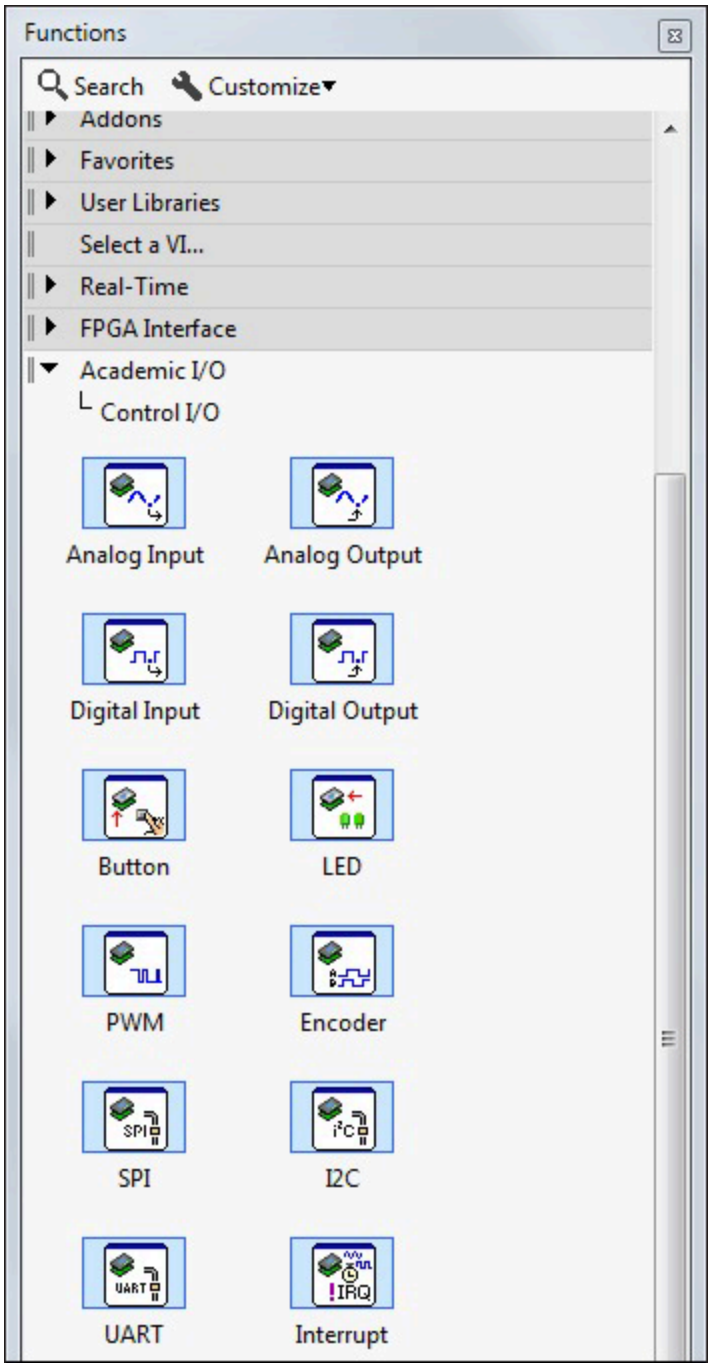
You can use LabVIEW Real-Time (RT) Express VIs, LabVIEW RT Low Level VIs, and LabVIEW FPGA I/O nodes to program the Analog Output channels.

Programming Examples

The LabVIEW ELVIS III Toolkit provides examples of using analog output channels to perform signal generation. You can find these examples in the `labview\examples\ELVIS III\Real-Time Control Applications\Analog IO\Analog IO.lvproj` directory.

LabVIEW RT Express VIs

Use the Express VIs to interactively configure the settings for the I/O channels. When you place an Express VI on the block diagram or double-click an Express VI, a configuration dialog box appears. Use this configuration dialog box to configure the Express VI. Find the Express VIs on the **Academic I/O** » **Control I/O** subpalette on the Functions palette, as shown in the following figure:

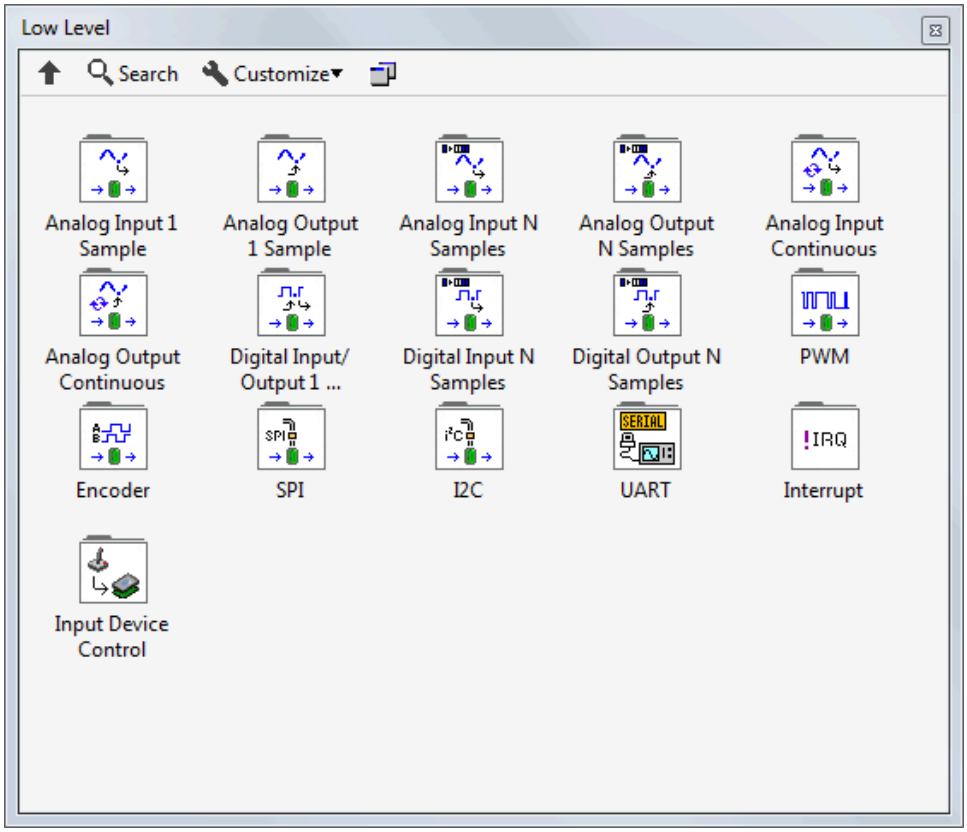


The LabVIEW ELVIS III Toolkit provides Analog Output Express VI to access the Analog Output channels.

LabVIEW RT Low Level VIs

Use the Low Level VIs to have more programmatic access to settings of I/O channels. For example, you can use the Low Level VIs to open or close certain channels and change the channel configuration at run time. Find the Low Level VIs on the Low Level

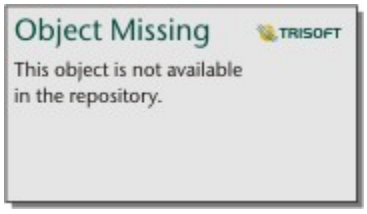
palette, as shown in the following figure:



The LabVIEW ELVIS III Toolkit provides the following Low Level VIs to access the Analog Output channels:

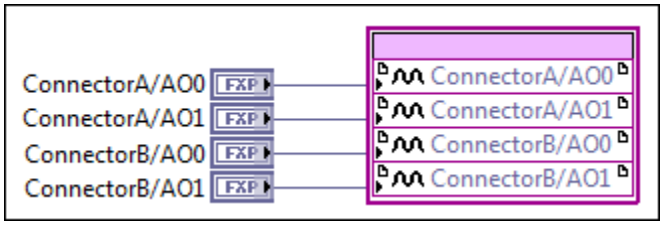
- Analog Output 1 Sample VIs
- Analog Output N Samples VIs
- Analog Output Continuous VIs

Select **Help** » **Show Context Help** or press <Ctrl-H> to display the Context Help window, from where you learn the basic information about each of the Express VIs and Low Level VIs. To learn more details about the VIs, refer to the ***LabVIEW ELVIS III Toolkit Help*** by clicking **Detailed help** at the bottom of the Context Help window, shown as follows:



LabVIEW FPGA I/O nodes

Use the FPGA I/O nodes from the FPGA palette to access the Analog Output channels on the NI ELVIS III. You can also use the FPGA I/O property nodes if needed. Channels from both banks on the NI ELVIS III can be used in a single FPGA I/O node. The I/O banks are denoted as connectors in the software. The following figure shows a VI that uses FPGA I/O nodes to generate outputs to AO channels 0 to 1 on Connector A and Connector B.



Refer to the **FPGA I/O Functions** section of the ***LabVIEW FPGA Module Help*** for detailed information about using the FPGA I/O nodes to perform operations on FPGA targets. Refer to the **NI ELVIS III** section in the ***NI Compact RIO Device Drivers Help*** to learn what terminals and I/O methods and properties you can access for the NI ELVIS III. You can access these help files by selecting **Help** » **LabVIEW Help** in LabVIEW, or search for their online versions on ni.com/manuals.

Analog Output Specifications

Specifications are ***Typical*** unless otherwise noted.

Number of channels	4, capable of independent operation
DAC Resolution	16 bits
Output range	±10 V

Maximum update rate	1.6 MS/s
Slew rate (100 pF load)	8.2 V/µs

Table 4. Analog Output Accuracy

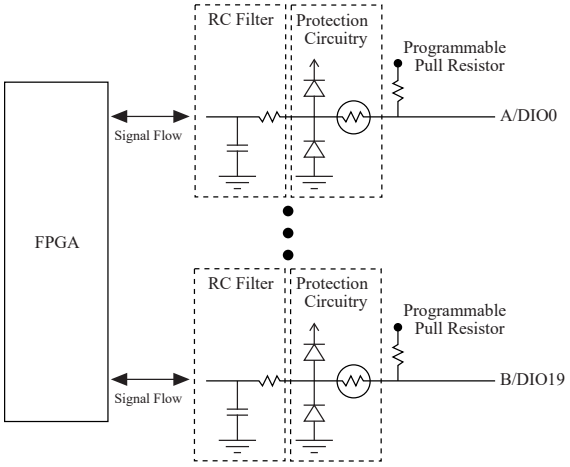
Measurement Conditions	Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Typical (25 °C ± 5 °C)	0.089%	0.029%
Maximum (10 °C to 35 °C)	0.430%	0.100%

Current drive	4 mA/channel maximum
Capacitive drive	3.3 nF
Output impedance	0.5 Ω
Protection	Short-circuit to ground
Power-on state[1]	0 V

Digital I/O

The digital I/O section consists of 40 channels of digital I/O. The basic I/O capabilities are identical across all 40 channels. Each has independent control over its input, output, and output enable.

Figure 8. Digital I/O Circuitry



Connecting Signals to Digital I/O

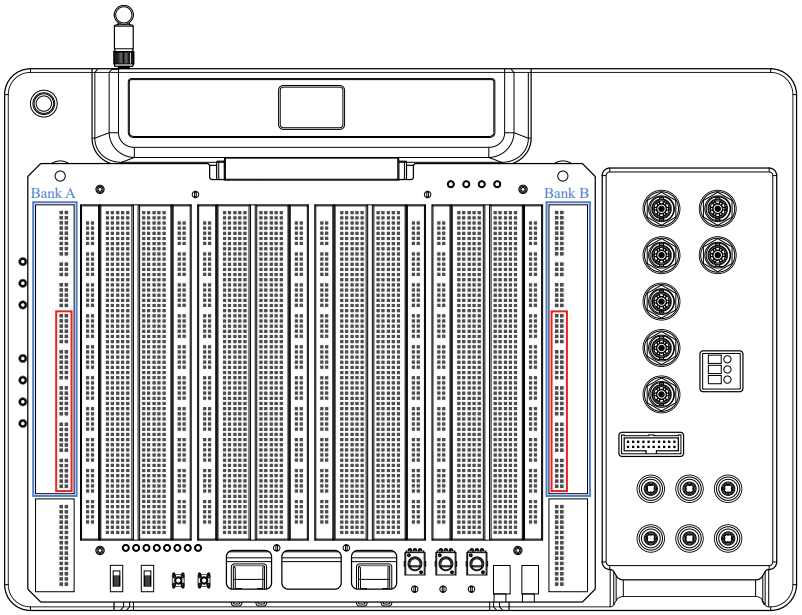
The digital lines can be configured as input or output. Each channel includes an RC filter, protection circuitry, and a programmable pull resistor. When an NI ELVIS III application board is detected, they are all automatically configured as pull-up resistors. The following table shows the channel mapping.

Table 5. Digital I/O Signal Mapping

Application Board Terminals		Signals
Bank A	A/DIO0, ..., A/DIO19	DIO 0, ..., DIO 19
Bank B	B/DIO0, ..., B/DIO19	DIO 0, ..., DIO 19
DGND		Digital Ground

Notice Use DGND for digital signals and power supplies only.

You can use the NI ELVIS III Prototyping Board to access these signals. The following diagram shows the NI ELVIS III with the digital I/O terminals highlighted.



Note The Digital I/O instrument does not use the DIO 16 - 19 terminals.

Programming Digital I/O with LabVIEW

You can use LabVIEW Real-Time (RT) Express VIs, LabVIEW RT Low Level VIs, and LabVIEW FPGA I/O nodes to program the Digital Input/Output channels. In particular, the LabVIEW ELVIS III Toolkit provides Express VIs and Low Level VIs that you can use to generate various types of digital signals, including I2C, PWM, SPI, and UART.

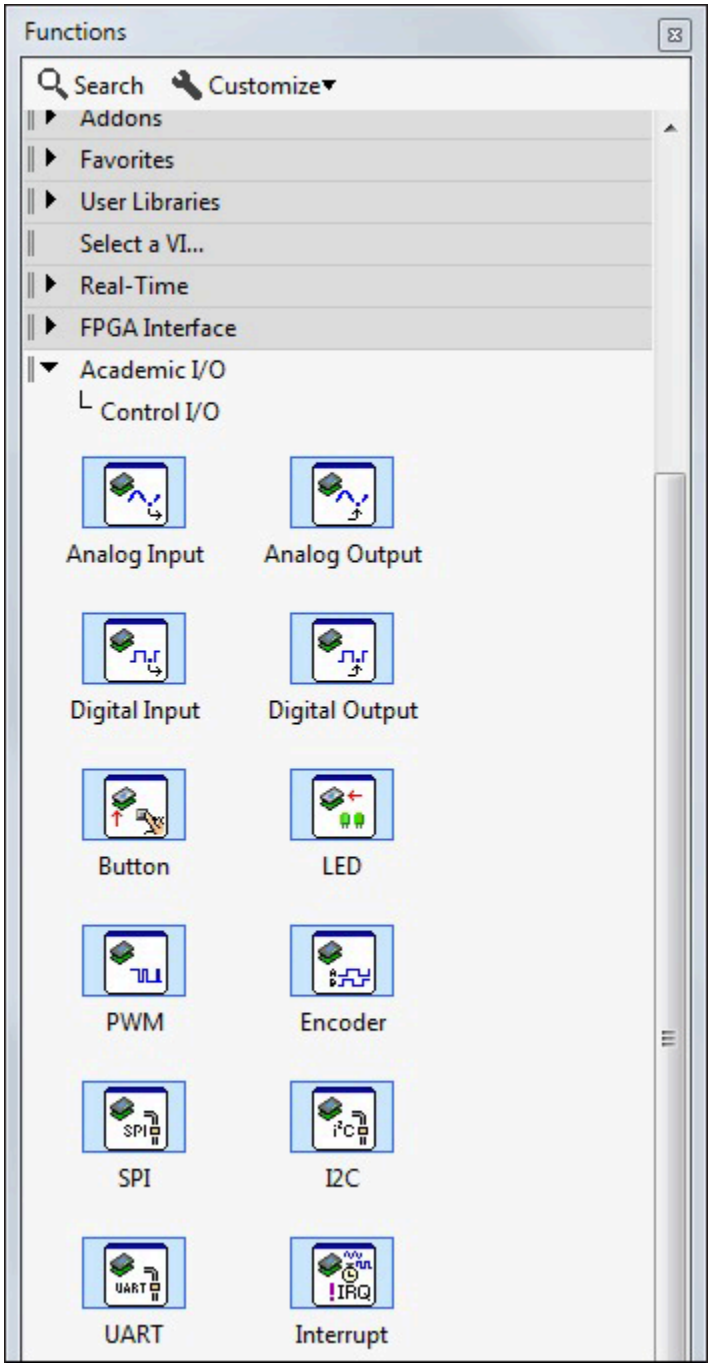
Programming Examples

The LabVIEW ELVIS III Toolkit provides examples of using digital input and output channels to perform signal acquisition and generation. You can find these examples in the `labview\examples\ELVIS III\Real-Time Control Applications\Digital IO\Digital IO.lvproj` directory.

LabVIEW RT Express VIs

Use the Express VIs to interactively configure the settings for the I/O channels. When you place an Express VI on the block diagram or double-click an Express VI, a configuration dialog box appears. Use this configuration dialog box to configure the Express VI. Find the Express VIs on the **Academic I/O** » **Control I/O** subpalette on the

Functions palette, as shown in the following figure:

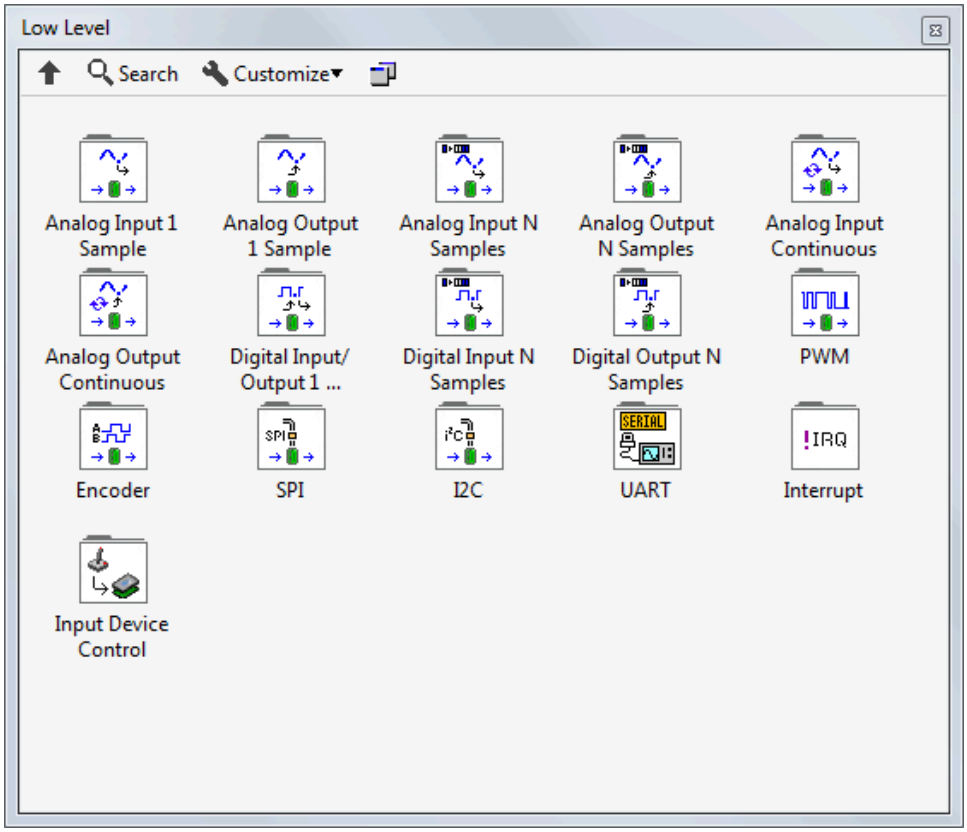


The LabVIEW ELVIS III Toolkit provides the following Express VIs to access the Digital Input/Output channels:

- Digital Input Express VI
- Digital Output Express VI

LabVIEW RT Low Level VIs

Use the Low Level VIs to have more programmatic access to settings of I/O channels. For example, you can use the Low Level VIs to open or close certain channels and change the channel configuration at run time. Find the Low Level VIs on the Low Level palette, as shown in the following figure:



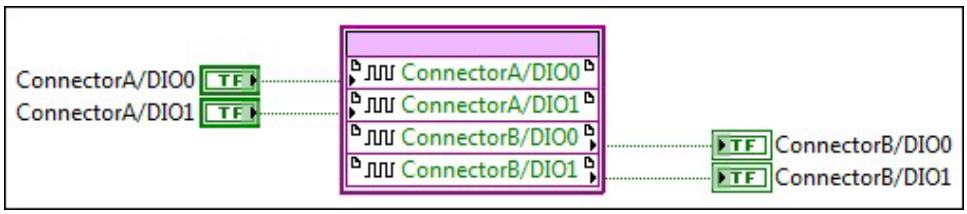
The LabVIEW ELVIS III Toolkit provides the following Low Level VIs to access the Digital Input/Output channels:

- Digital Input/Output 1 Sample VIs
- Digital Input N Samples VIs
- Digital Output N Samples VIs

Select **Help** » **Show Context Help** or press <Ctrl-H> to display the Context Help window, from where you learn the basic information about each of the Express VIs and Low Level VIs. To learn more details about the VIs, refer to the ***LabVIEW ELVIS III Toolkit Help*** by clicking **Detailed help** at the bottom of the Context Help window, shown as follows:

LabVIEW FPGA I/O nodes

Use the FPGA I/O nodes from the FPGA palette to access the Digital Input/Output channels on the NI ELVIS III. You can also use the FPGA I/O property nodes if needed. Channels from both banks on the NI ELVIS III can be used in a single FPGA I/O node. The I/O banks are denoted as connectors in the software. The following figure shows a VI that uses FPGA I/O nodes to generate outputs to DIO channels 0 to 1 on Connector A and read inputs from DIO channels 0 to 1 on Connector B.



Refer to the **FPGA I/O Functions** section of the ***LabVIEW FPGA Module Help*** for detailed information about using the FPGA I/O nodes to perform operations on FPGA targets. Refer to the **NI ELVIS III** section in the ***NI Compact RIO Device Drivers Help*** to learn what terminals and I/O methods and properties you can access for the NI ELVIS III. You can access these help files by selecting **Help** » **LabVIEW Help** in LabVIEW, or search for their online versions on ni.com/manuals.

Digital I/O Specifications

Specifications are ***Typical*** unless otherwise noted.

Number of DIO channels	40

Direction control	Individually programmable as input or output
Logic level	5 V compatible LVTTL input; 3.3 V LVTTL output
Pull-up/down	40.2 kΩ pull-up to 3.3 V[1]
Protection	±30 V
Input logic levels	
Input low voltage, V_{IL}	
Minimum	0 V
Maximum	0.8 V
Input high voltage, V_{IH}	
Minimum	2.0 V
Maximum	5.25 V
Output logic levels	
Output low voltage, V_{OL} sinking 4 mA	
Minimum	0 V
Maximum	0.4 V
Output high voltage, V_{OH} sourcing 4 mA	

Minimum	2.4 V
Maximum	3.465 V
Minimum output pulse width	20 ns
Maximum frequencies for secondary digital functions	
SPI	4 MHz
PWM	100 kHz
Quadrature encoder input	100 kHz
I^2C	400 kHz [2]
UART lines	
Maximum baud rate	230,400 bps
Data bits	5, 6, 7, 8
Stop bits	1, 2
Parity	Odd, Even, Mark, Space
Flow control	XON/XOFF

Fixed User Power Supplies

The fixed user power supplies section consists of four power rails (+15 V, -15 V, +5 V, and +3.3 V).

Connecting Signals to Fixed User Power Supplies

All power supplies on the NI ELVIS III are referenced to ground.

Notice Use DGND for digital signals and power supplies only.

Note All fixed user power supply rails will be turned off automatically if two or more power rails are in a short circuit condition. To restore functionality of the fixed user power supplies, the faults must be removed and the power re-enabled by pressing the application board power button on the workstation.

Note The power up and power down sequences across the fixed power supplies are not guaranteed

Refer to the NI ELVIS III Prototyping Board section on how to access these signals on the NI ELVIS III prototyping board.

Programming Options

The Fixed User Power Supplies channels are not programmable.

Fixed User Power Supplies Specifications

Specifications are ***Typical*** unless otherwise noted.

Notice Exceeding the power limits may cause unpredictable device behavior.

+15 V power output	
Output voltage (no load)	+15 V ± 5%
Maximum current	500 mA [1]
Ripple and noise (20 MHz bandwidth)	150 mV peak-to-peak maximum
Protection	Short-circuit to ground
-15 V power output	
Output voltage (no load)	-15 V ± 5%
Maximum current	-500 mA [1]
Ripple and noise (20 MHz bandwidth)	150 mV peak-to-peak maximum
Protection	Short-circuit to ground
+5 V power output	
Output voltage (no load)	+5 V ± 5%
Maximum current	2 A [1]
Ripple and noise (20 MHz bandwidth)	50 mV peak-to-peak maximum

Protection	Short-circuit to ground
+3.3 V power output	
Output voltage (no load)	+3.3 V ± 5%
Maximum current	310 mA [1]
Ripple and noise (20 MHz bandwidth)	33 mV peak-to-peak maximum
Protection	Short-circuit to ground